45. Management Data Input/Output (MDIO) Interface

45.1 Overview

This clause defines the logical and electrical characteristics of an extension to the two signal Management Data Input/Output (MDIO) Interface specified in Clause 22.

The purpose of this extension is to provide the ability to access more device registers while still retaining logical compatibility with the MDIO interface defined in Clause 22. Clause 22 specifies the MDIO frame format and uses an ST code of 01 to access registers. In this clause, additional registers are added to the address space by defining MDIO frames that use an ST code of 00.

This extension to the MDIO interface is applicable to the following:

— Implementations that operate at speeds of 10 Gb/s and above.
— Implementations of 10PASS-TS and 2BASE-TL subscriber network Physical layer devices.
— Implementations of 10, 100, or 1000 Mb/s with additional management functions beyond those defined in Clause 22.

The MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

Throughout this clause, an “a.b.c” format is used to identify register bits, where “a” is the device address, “b” is the register address, and “c” is the bit number within the register.

45.1.1 Summary of major concepts

The following are major concepts of the MDIO Interface:

a) Preserve the management frame structure defined in 22.2.4.5.
b) Define a mechanism to address more registers than specified in 22.2.4.5.
c) Define ST and OP codes to identify and control the extended access functions.
d) Provide an electrical interface specification that is compatible with common digital CMOS ASIC processes.

45.1.2 Application

This clause defines a management interface between Station Management (STA) and the sublayers that form a Physical Layer device (PHY) entity. Where a sublayer, or grouping of sublayers, is an individually manageable entity, it is known as an MDIO Manageable Device (MMD). This clause allows a single STA, through a single MDIO interface, to access up to 32 PHYs (defined as PRTAD in the frame format defined in 45.3) consisting of up to 32 MMDs as shown in Figure 45–1. The MDIO interface can support up to a maximum of 65 536 registers in each MMD.

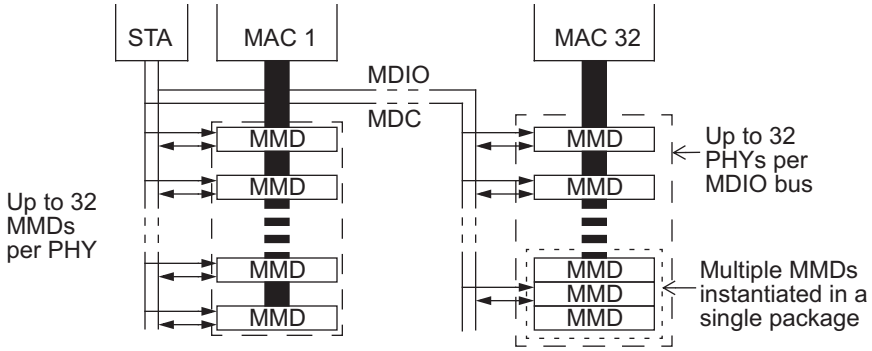

Figure 45–1—DTE and MMD devices

45.2 MDIO Interface Registers

The management interface specified in Clause 22 provides a simple, two signal, serial interface to connect a Station Management entity and a managed PHY for providing access to management parameters and services. The interface is referred to as the MII management interface.

The MDIO interface is based on the MII management interface, but differs from it in several ways. The MDIO interface uses indirect addressing to create an extended address space allowing a much larger number of registers to be accessed within each MMD. The MDIO address space is orthogonal to the MII management interface address space. The mechanism for the addressing is defined in 45.3. The MDIO electrical interface operates at lower voltages than those specified for the MII management interface. The electrical interface is specified in 45.4. For cases where a single entity combines Clause 45 MMDs with Clause 22 registers, then the Clause 22 registers may be accessed using the Clause 45 electrical interface and the Clause 22 management frame structure. The list of possible MMDs is shown in Table 45–1. The PHY XS and DTE XS devices are the two partner devices used to extend the interface that sits immediately below the Reconciliation Sublayer. For 10 Gigabit Ethernet, the interface extenders are defined as the XGXS devices. For 10PASS-TS and 2BASE-TL, control and monitoring of the TC sublayer is defined in the TC MMD. For 10, 100 and 1000 Mb/s PHYs, further management capability is defined in the Clause 22 extension MMD.

10PASS-TS and 2BASE-TL each have two port subtypes, 10PASS-TS-O, 10PASS-TS-R, 2BASE-TL-O and 2BASE-TL-R. Hereafter, referred to generically as -O and -R. The -O subtype corresponds to the port located at the service provider end of a subscriber link (the central office end). The -R subtype corresponds to the port located at the subscriber end of a subscriber link (the remote end). See 61.1 for more information.

Some register behaviour may differ based on the port subtype. In the case where a register's behaviour or definition differs between port subtypes, it is noted in the register description and in the bit definition tables (denoted by "O:" and "R:" in the R/W column).

The Clause 22 extension MMD allows new features to be added to 10, 100, and 1000 Mb/s PHYs beyond those already defined in Clause 22.

If a device supports the MDIO interface it shall respond to all possible register addresses for the device and return a value of zero for undefined and unsupported registers. Writes to undefined registers and read-only

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6	TC
7 through 28	Reserved
29	Clause 22 extension
30	Vendor specific 1
31	Vendor specific 2

registers shall have no effect. The operation of an MMD shall not be affected by writes to reserved and unsupported register bits, and such register bits shall return a value of zero when read.

In the case of two registers that together form a 32-bit counter, whenever the most significant 16-bit register of the counter is read, the 32-bit counter value is latched into the register pair, the value being latched before the contents of the most significant 16 bits are driven on the MDIO interface and the contents of both registers is cleared to all zeros. A subsequent read from the least significant 16-bit register will return the least significant 16 bits of the latched value, but will not change the contents of the register pair. Writing to these registers has no effect. Counters that adhere to this behaviour are marked in their bit definition tables with the tag “MW = Multi-word”.

To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of zero and ignore reserved bits on read.

Some of the bits within MMD registers are defined as latching low (LL) or latching high (LH). When a bit is defined as latching low and the condition for the bit to be low has occurred, the bit shall remain low until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors. When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

For multi-bit fields, the lowest numbered bit of the field in the register corresponds to the least significant bit of the field.

Figure 45–2 describes the signal terminology used for the MMDs.

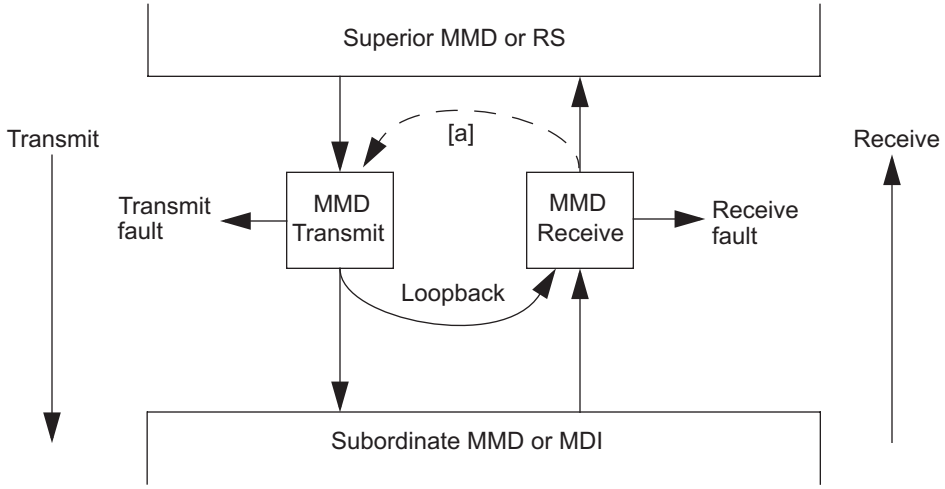

Figure 45–2—MMD signal terminology

[a] Direction of the optional PHY XS loopback

Each MMD contains registers 5 and 6, as defined in Table 45–2. Bits read as a one in this register indicate which MMDs are instantiated within the same package as the MMD being accessed. Bit 5.0 is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. Bit 6.13 indicates that Clause 22 functionality is extended using the Clause 45 electrical interface through MMD 29. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

Table 45–2—Devices in package registers bit definitions

Bit(s)[a]	Name	Description	R/W[b]
m.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
m.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
m.6.13	Clause 22 extension present	1 = Clause 22 extension present in package 0 = Clause 22 extension not present in package	RO
m.6.12:0	Reserved	Ignore on read	RO
m.5.15:7	Reserved	Ignore on read	RO
m.5.6	TC present	1 = TC present in package 0 = TC not present in package	RO
m.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
m.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
m.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
m.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
m.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
m.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]m = address of MMD accessed (see Table 45–1)
[b]RO = Read Only

45.2.1 PMA/PMD registers

The assignment of registers in the PMA/PMD is shown in Table 45–3.

Table 45–3—PMA/PMD registers

Register address	Register name
1.0	PMA/PMD control 1
1.1	PMA/PMD status 1
1.2, 1.3	PMA/PMD device identifier
1.4	PMA/PMD speed ability
1.5, 1.6	PMA/PMD devices in package
1.7	10G PMA/PMD control 2
1.8	10G PMA/PMD status 2
1.9	10G PMD transmit disable
1.10	10G PMD receive signal detect
1.11	10G PMA/PMD extended ability register
1.12, 1.13	Reserved
1.14, 1.15	PMA/PMD package identifier
1.16 through 1.29	
1.30	10P/2B PMA/PMD control
1.31	10P/2B PMA/PMD status
1.32	10P/2B link partner PMA/PMD control[a]
1.33	10P/2B link partner PMA/PMD status[a]
1.34, 1.35	Reserved
1.36	10P/2B link loss counter
1.37	10P/2B RX SNR margin
1.38	10P/2B link partner RX SNR margin[a]
1.39	10P/2B line attenuation
1.40	10P/2B link partner line attenuation[a]
1.41	10P/2B line quality thresholds
1.42	2B link partner line quality thresholds[a]
1.43	10P FEC correctable errors counter
1.44	10P FEC uncorrectable errors counter
1.45	10P link partner FEC correctable errors[a]
1.46	10P link partner FEC uncorrectable errors[a]
1.47	10P electrical length
1.48	10P link partner electrical length[a]
1.49	10P PMA/PMD general configuration[a]
1.50	10P PSD configuration[a]
1.51, 1.52	10P downstream data rate configuration[a]
1.53	10P downstream Reed-Solomon configuration[a]

Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name
1.54, 1.55	10P upstream data rate[a]
1.56	10P upstream Reed-Solomon configuration[a]
1.57, 1.58	10P tone group
1.59, 1.60, 1.61, 1.62, 1.63	10P tone control parameters[a]
1.64	10P tone control action[a]
1.65, 1.66, 1.67	10P tone status
1.68	10P outgoing indicator bits
1.69	10P incoming indicator bits
1.70	10P cyclic extension configuration
1.71	10P attainable downstream data rate
1.72 through 1.79	Reserved
1.80	2B general parameter
1.81 through 1.88	2B PMD parameters
1.89	2B code violation errors counter
1.90	2B link partner code violation errors[a]
1.91	2B errored seconds counter
1.92	2B link partner errored seconds[a]
1.93	2B severely errored seconds counter
1.94	2B link partner severely errored seconds[a]
1.95	2B LOSW counter
1.96	2B link partner LOSW[a]
1.97	2B unavailable seconds counter
1.98	2B link partner unavailable seconds[a]
1.99	2B state defects
1.100	2B link partner state defects[a]
1.101	2B negotiated constellation
1.102 through 1.109	2B extended PMD parameters
1.110 through 1.32 767	Reserved
1.32 768 through 1.65 535	Vendor specific

[a]Register is defined only for -O port types and is reserved for -R ports.

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

The assignment of bits in the PMA/PMD control 1 register is shown in Table 45–4. The default value for each bit of the PMA/PMD control 1 register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.0.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC
1.0.14	Reserved	Value always 0, writes ignored	R/W
1.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
1.0.12	Reserved	Value always 0, writes ignored	R/W
1.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
1.0.10:7	Reserved	Value always 0, writes ignored	R/W
1.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
1.0.1	Reserved	Value always 0, writes ignored	R/W
1.0.0	PMA loopback	1 = Enable PMA loopback mode 0 = Disable PMA loopback mode	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.1.1 Reset (1.0.15)

Resetting a PMA/PMD is accomplished by setting bit 1.0.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PMA/PMD shall return a value of one in bit 1.0.15 when a reset is in progress; otherwise, it shall return a value of zero. A PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.0.15. During a reset, a PMD/PMA shall respond to reads from register bits 1.0.15 and 1.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset or low-power mode.

45.2.1.1.2 Low power (1.0.11)

A PMA/PMD may be placed into a low-power mode by setting bit 1.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PMA/PMD. The behavior of the PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.0.11 is zero.

NOTE—This operation will interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset or low-power mode.

45.2.1.1.3 Speed selection (1.0.13,1.0.6, 1.0.5:2)

Speed selection bits 1.0.13 and 1.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PMA/PMD may be selected using bits 5 through 2. The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. A PMA/PMD may ignore writes to the PMA/PMD speed selection bits that select speeds it has not advertised in the PMA/PMD speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD speed selection defaults to a supported ability.

When set to 0001, bits 5:2 select the use of the 10PASS-TS or 2BASE-TL PMA/PMD. More specific mode selection is performed using the 10P/2B PMA control register (45.2.1.12).

45.2.1.1.4 PMA loopback (1.0.0)

The PMA shall be placed in a loopback mode of operation when bit 1.0.0 is set to a one. When bit 1.0.0 is set to a one, the PMA shall accept data on the transmit path and return it on the receive path.

The loopback function is mandatory for the 10GBASE-X port type and optional for all other port types, except 2BASE-TL and 10PASS-TS, which do not support loopback. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the loopback function shall ignore writes to this bit and shall return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and 51.8, and the loopback ability bit is specified in the 10G PMA/PMD status 2 register.

The default value of bit 1.0.0 is zero.

NOTE—The signal path through the PMA that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PMA circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

The assignment of bits in the PMA/PMD status 1 register is shown in Table 45–5. All the bits in the PMA/PMD status 1 register are read only; therefore, a write to the PMA/PMD status 1 register shall have no effect.

Table 45–5—PMA/PMD status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1.15:8	Reserved	Ignore when read	RO
1.1.7	Fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.1.6:3	Reserved	Ignore when read	RO
1.1.2	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL
1.1.1	Low-power ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	RO
1.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

45.2.1.2.1 Fault (1.1.7)

Fault is a global PMA/PMD variable. When read as a one, bit 1.1.7 indicates that either (or both) the PMA or the PMD has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 1.1.7 indicates that neither the PMA nor the PMD has detected a fault condition. For 10 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one. For 10PASS-TS or 2BASE-TL operations, when read as a one, a fault has been detected and more detailed information is conveyed in 45.2.1.16, 45.2.1.39, 45.2.1.40, and 45.2.1.55.

45.2.1.2.2 Receive link status (1.1.2)

When read as a one, bit 1.1.2 indicates that the PMA/PMD receive link is up. When read as a zero, bit 1.1.2 indicates that the PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior.

While a 10PASS-TS or 2BASE-TL PMA/PMD is initializing, this bit shall indicate receive link down (see 45.2.1.13).

45.2.1.2.3 Low-power ability (1.1.1)

When read as a one, bit 1.1.1 indicates that the PMA/PMD supports the low-power feature. When read as a zero, bit 1.1.1 indicates that the PMA/PMD does not support the low-power feature. If a PMA/PMD supports the low-power feature, then it is controlled using the low-power bit 1.0.11.

45.2.1.3 PMA/PMD device identifier (Registers 1.2 and 1.3)

Registers 1.2 and 1.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PMA/PMD. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number.

A PMA/PMD may return a value of zero in each of the 32 bits of the PMA/PMD device identifier to indicate that a unique identifier as described above is not provided.

The format of the PMA/PMD device identifier is specified in 22.2.4.3.1.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

The assignment of bits in the PMA/PMD speed ability register is shown in Table 45–6.

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.4.15:3	Reserved for future speeds	Value always 0, writes ignored	RO
1.4.2	10PASS-TS capable	1 = PMA/PMD is capable of operating as 10PASS-TS 0 = PMA/PMD is not capable of operating as 10PASS-TS	RO
1.4.1	2BASE-TL capable	1 = PMA/PMD is capable of operating as 2BASE-TL 0 = PMA/PMD is not capable of operating as 2BASE-TL	RO
1.4.0	10G capable	1 = PMA/PMD is capable of operating at 10 Gb/s 0 = PMA/PMD is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.1.4.1 10PASS-TS capable (1.4.2)

When read as a one, bit 1.4.2 indicates that the PMA/PMD is able to operate as 10PASS-TS. When read as a zero, bit 1.4.2 indicates that the PMA/PMD is not able to operate as 10PASS-TS.

45.2.1.4.2 2BASE-TL capable (1.4.1)

When read as a one, bit 1.4.1 indicates that the PMA/PMD is able to operate as 2BASE-TL. When read as a zero, bit 1.4.1 indicates that the PMA/PMD is not able to operate as 2BASE-TL.

45.2.1.4.3 10G capable (1.4.0)

When read as a one, bit 1.4.0 indicates that the PMA/PMD is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 1.4.0 indicates that the PMA/PMD is not able to operate at a data rate of 10 Gb/s.

45.2.1.5 PMA/PMD devices in package (Registers 1.5 and 1.6)

The PMA/PMD devices in package registers are defined in Table 45–2.

45.2.1.6 10G PMA/PMD control 2 register (Register 1.7)

The assignment of bits in the 10G PMA/PMD control 2 register is shown in Table 45–7.

Table 45–7—10G PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:3	Reserved	Value always 0, writes ignored	R/W
1.7.2:0	PMA/PMD type selection	2 1 0 1 1 1 = 10GBASE-SR PMA/PMD type 1 1 0 = 10GBASE-LR PMA/PMD type 1 0 1 = 10GBASE-ER PMA/PMD type 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 1 1 = 10GBASE-SW PMA/PMD type 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 = 10GBASE-CX4 PMA/PMD type	R/W

[a]R/W = Read/Write

45.2.1.6.1 PMA/PMD type selection (1.7.2:0)

The PMA/PMD type of the 10G PMA/PMD shall be selected using bits 2 through 0. The PMA/PMD type abilities of the 10G PMA/PMD are advertised in bits 9 and 7 through 0 of the 10G PMA/PMD status 2 register and bit 0 of the 10G PMA/PMD extended ability register. A 10G PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised in the status register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD type selection defaults to a supported ability.

45.2.1.7 10G PMA/PMD status 2 register (Register 1.8)

The assignment of bits in the 10G PMA/PMD status 2 register is shown in Table 45–8. All the bits in the 10G PMA/PMD status 2 register are read only; a write to the 10G PMA/PMD status 2 register shall have no effect.

Table 45–8—10G PMA/PMD status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
1.8.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO
1.8.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
1.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
1.8.9	Extended abilities	1 = PMA/PMD has extended abilities listed in register 1.11 0 = PMA/PMD does not have extended abilities	RO
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO
1.8.7	10GBASE-SR ability	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR	RO
1.8.6	10GBASE-LR ability	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR	RO
1.8.5	10GBASE-ER ability	1 = PMA/PMD is able to perform 10GBASE-ER 0 = PMA/PMD is not able to perform 10GBASE-ER	RO
1.8.4	10GBASE-LX4 ability	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4	RO
1.8.3	10GBASE-SW ability	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW	RO
1.8.2	10GBASE-LW ability	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW	RO
1.8.1	10GBASE-EW ability	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW	RO
1.8.0	PMA loopback ability	1 = PMA has the ability to perform a loopback function 0 = PMA does not have the ability to perform a loopback function	RO

[a]RO = Read Only, LH = Latching High

45.2.1.7.1 Device present (1.8.15:14)

When read as <10>, bits 1.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 1.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.1.7.2 Transmit fault ability (1.8.13)

When read as a one, bit 1.8.13 indicates that the PMA/PMD has the ability to detect a fault condition on the transmit path. When read as a zero, bit 1.8.13 indicates that the PMA/PMD does not have the ability to detect a fault condition on the transmit path.

45.2.1.7.3 Receive fault ability (1.8.12)

When read as a one, bit 1.8.12 indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.8.12 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.7.4 Transmit fault (1.8.11)

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for serial PMDs is given in 52.4.8. The description of the transmit fault function for WWDM PMDs is given in 53.4.10. The description of the transmit fault function for the 10GBASE-CX4 PMD is given in 54.5.10. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.11 is zero.

45.2.1.7.5 Receive fault (1.8.10)

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for serial PMDs is given in 52.4.9. The description of the receive fault function for WWDM PMDs is given in 53.4.11. The description of the receive fault function for the 10GBASE-CX4 PMD is given in 54.5.11. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.10 is zero.

45.2.1.7.6 PMA/PMD extended abilities (1.8.9)

When read as a one, bit 1.8.9 indicates that the PMA/PMD has extended abilities listed in register 1.11. When read as a zero, bit 1.8.9 indicates that the PMA/PMD does not have extended abilities.

45.2.1.7.7 PMD transmit disable ability (1.8.8)

When read as a one, bit 1.8.8 indicates that the PMD is able to perform the transmit disable function. When read as a zero, bit 1.8.8 indicates that the PMD is not able to perform the transmit disable function. If a PMD is able to perform the transmit disable function, then it is controlled using the PMD transmit disable register.

45.2.1.7.8 10GBASE-SR ability (1.8.7)

When read as a one, bit 1.8.7 indicates that the PMA/PMD is able to support a 10GBASE-SR PMA/PMD type. When read as a zero, bit 1.8.7 indicates that the PMA/PMD is not able to support a 10GBASE-SR PMA/PMD type.

45.2.1.7.9 10GBASE-LR ability (1.8.6)

When read as a one, bit 1.8.6 indicates that the PMA/PMD is able to support a 10GBASE-LR PMA/PMD type. When read as a zero, bit 1.8.6 indicates that the PMA/PMD is not able to support a 10GBASE-LR PMA/PMD type.

45.2.1.7.10 10GBASE-ER ability (1.8.5)

When read as a one, bit 1.8.5 indicates that the PMA/PMD is able to support a 10GBASE-ER PMA/PMD type. When read as a zero, bit 1.8.5 indicates that the PMA/PMD is not able to support a 10GBASE-ER PMA/PMD type.

45.2.1.7.11 10GBASE-LX4 ability (1.8.4)

When read as a one, bit 1.8.4 indicates that the PMA/PMD is able to support a 10GBASE-LX4 PMA/PMD type. When read as a zero, bit 1.8.4 indicates that the PMA/PMD is not able to support a 10GBASE-LX4 PMA/PMD type.

45.2.1.7.12 10GBASE-SW ability (1.8.3)

When read as a one, bit 1.8.3 indicates that the PMA/PMD is able to support a 10GBASE-SW PMA/PMD type. When read as a zero, bit 1.8.3 indicates that the PMA/PMD is not able to support a 10GBASE-SW PMA/PMD type.

45.2.1.7.13 10GBASE-LW ability (1.8.2)

When read as a one, bit 1.8.2 indicates that the PMA/PMD is able to support a 10GBASE-LW PMA/PMD type. When read as a zero, bit 1.8.2 indicates that the PMA/PMD is not able to support a 10GBASE-LW PMA/PMD type.

45.2.1.7.14 10GBASE-EW ability (1.8.1)

When read as a one, bit 1.8.1 indicates that the PMA/PMD is able to support a 10GBASE-EW PMA/PMD type. When read as a zero, bit 1.8.1 indicates that the PMA/PMD is not able to support a 10GBASE-EW PMA/PMD type.

45.2.1.7.15 PMA loopback ability (1.8.0)

When read as a one, bit 1.8.0 indicates that the PMA is able to perform the loopback function. When read as a zero, bit 1.8.0 indicates that the PMA is not able to perform the loopback function. If a PMA is able to perform the loopback function, then it is controlled using the PMA loopback bit 1.0.0.

45.2.1.8 10G PMD transmit disable register (Register 1.9)

The assignment of bits in the 10G PMD transmit disable register is shown in Table 45–9. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the 10G PMD transmit disable register and may return a value of zero for all bits.

A PMD device that operates using a single wavelength and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bits 1.9.4:1 and return a value of zero for those bits when they are read. The transmit disable function for serial PMDs is described in 52.4.7. The transmit disable function for wide wavelength division multiplexing (WWDM) PMDs is described in 53.4.7. The transmit disable function for four-lane electrical PMDs is described in 54.5.6.

Table 45–9—10G PMD transmit disable register bit definitions

Bit(s)	Name	Description	R/W[a]
1.9.15:5	Reserved	Value always 0, writes ignored	R/W
1.9.4	PMD transmit disable 3	1 = Disable output on transmit lane 3 0 = Enable output on transmit lane 3	R/W
1.9.3	PMD transmit disable 2	1 = Disable output on transmit lane 2 0 = Enable output on transmit lane 2	R/W
1.9.2	PMD transmit disable 1	1 = Disable output on transmit lane 1 0 = Enable output on transmit lane 1	R/W
1.9.1	PMD transmit disable 0	1 = Disable output on transmit lane 0 0 = Enable output on transmit lane 0	R/W
1.9.0	Global PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

[a]R/W = Read/Write

45.2.1.8.1 PMD transmit disable 3 (1.9.4)

When bit 1.9.4 is set to a one, the PMD shall disable output on lane 3 of the transmit path. When bit 1.9.4 is set to a zero, the PMD shall enable output on lane 3 of the transmit path.

The default value for bit 1.9.4 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.2 PMD transmit disable 2 (1.9.3)

When bit 1.9.3 is set to a one, the PMD shall disable output on lane 2 of the transmit path. When bit 1.9.3 is set to a zero, the PMD shall enable output on lane 2 of the transmit path.

The default value for bit 1.9.3 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.3 PMD transmit disable 1 (1.9.2)

When bit 1.9.2 is set to a one, the PMD shall disable output on lane 1 of the transmit path. When bit 1.9.2 is set to a zero, the PMD shall enable output on lane 1 of the transmit path.

The default value for bit 1.9.2 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.4 PMD transmit disable 0 (1.9.1)

When bit 1.9.1 is set to a one, the PMD shall disable output on lane 0 of the transmit path. When bit 1.9.1 is set to a zero, the PMD shall enable output on lane 0 of the transmit path.

The default value for bit 1.9.1 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.5 Global PMD transmit disable (1.9.0)

When bit 1.9.0 is set to a one, the PMD shall disable output on the transmit path. When bit 1.9.0 is set to a zero, the PMD shall enable output on the transmit path.

For single wavelength PMD types, transmission will be disabled when this bit is set to one. When this bit is set to zero, transmission is enabled.

For multiple wavelength or lane PMD types, transmission will be disabled on all lanes when this bit is set to one. When this bit is set to zero, the lanes are individually controlled by their corresponding transmit disable bits 1.9.4:1.

The default value for bit 1.9.0 is zero.

45.2.1.9 10G PMD receive signal detect register (Register 1.10)

The assignment of bits in the 10G PMD receive signal detect register is shown in Table 45–10. The 10G PMD receive signal detect register is mandatory. PMD types that use only a single wavelength indicate the status of the receive signal detect using bit 1.10.0 and return a value of zero for bits 1.10.4:1. PMD types that use multiple wavelengths or lanes indicate the status of each lane in bits 1.10.4:1 and the logical AND of those bits in bit 1.10.0.

45.2.1.9.1 PMD receive signal detect 3 (1.10.4)

When bit 1.10.4 is read as a one, a signal has been detected on lane 3 of the PMD receive path. When bit 1.10.4 is read as a zero, a signal has not been detected on lane 3 of the PMD receive path.

45.2.1.9.2 PMD receive signal detect 2 (1.10.3)

When bit 1.10.3 is read as a one, a signal has been detected on lane 2 of the PMD receive path. When bit 1.10.3 is read as a zero, a signal has not been detected on lane 2 of the PMD receive path.

45.2.1.9.3 PMD receive signal detect 1 (1.10.2)

When bit 1.10.2 is read as a one, a signal has been detected on lane 1 of the PMD receive path. When bit 1.10.2 is read as a zero, a signal has not been detected on lane 1 of the PMD receive path.

Table 45–10—10G PMD receive signal detect register bit definitions

Bit(s)	Name	Description	R/W[a]
1.10.15:5	Reserved	Value always 0, writes ignored	RO
1.10.4	PMD receive signal detect 3	1 = Signal detected on receive lane 3 0 = Signal not detected on receive lane 3	RO
1.10.3	PMD receive signal detect 2	1 = Signal detected on receive lane 2 0 = Signal not detected on receive lane 2	RO
1.10.2	PMD receive signal detect 1	1 = Signal detected on receive lane 1 0 = Signal not detected on receive lane 1	RO
1.10.1	PMD receive signal detect 0	1 = Signal detected on receive lane 0 0 = Signal not detected on receive lane 0	RO
1.10.0	Global PMD receive signal detect	1 = Signal detected on receive 0 = Signal not detected on receive	RO

[a]RO = Read Only

45.2.1.9.4 PMD receive signal detect 0 (1.10.1)

When bit 1.10.1 is read as a one, a signal has been detected on lane 0 of the PMD receive path. When bit 1.10.1 is read as a zero, a signal has not been detected on lane 0 of the PMD receive path.

45.2.1.9.5 Global PMD receive signal detect (1.10.0)

When bit 1.10.0 is read as a one, a signal has been detected on all the PMD receive paths. When bit 1.10.0 is read as a zero, a signal has not been detected on at least one of the PMD receive paths.

Single wavelength PMD types indicate the status of their receive path signal using this bit.

Multiple wavelength or multiple lane PMD types indicate the global status of the lane-by-lane signal detect indications using this bit. This bit is read as a one when all the lane signal detect indications are one; otherwise, this bit is read as a zero.

45.2.1.10 10G PMA/PMD extended ability register (Register 1.11)

The assignment of bits in the 10G PMA/PMD extended ability register is shown in Table 45–11. All of the bits in the 10G PMA/PMD extended ability register are read only; a write to the 10G PMA/PMD extended ability register shall have no effect.

Table 45–11—10G PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.15:1	Reserved	Ignore on read	RO
1.11.0	10GBASE-CX4 ability	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO

[a]RO = Read Only

45.2.1.11 PMA/PMD package identifier (Registers 1.14 and 1.15)

Registers 1.14 and 1.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PMA/PMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PMA/PMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

45.2.1.12 10P/2B PMA/PMD control register (Register 1.30)

The assignment of bits in the 10P/2B PMA control register is shown in Table 45–12.

Table 45–12—10P/2B PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.30.15	PMA/PMD link control	1 = begin initialization, enable link (-R default) 0 = force link down (-O default)	R/W
1.30.14	STFU	Silence the far unit 1 = send silence command 0 = silence command inactive (default)	R/W
1.30.13:8	Silence time	Silence time = 10 × (value of bits + 1) seconds	R/W
1.30.7	Port subtype select	1 = port operates as an -O subtype 0 = port operates as a -R subtype	R/W
1.30.6	Handshake cleardown	1 = send cleardown command 0 = idle (default)	R/W, SC
1.30.5	Ignore incoming handshake	1 = PMA/PMD does not respond to handshake tones 0 = PMA/PMD responds to handshake tones	R/W
1.30.4:0	PMA/PMD type selection	4 3 2 1 0 0 0 0 0 0 = 10PASS-TS PMA/PMD type 0 0 0 0 1 = 2BASE-TL PMA/PMD type 0 0 0 1 0 = 2BASE-TL or 10PASS-TS (-R only) 0 0 0 1 1 = 2BASE-TL preferred, or 10PASS-TS (-O only) 0 0 1 0 0 = 10PASS-TS preferred, or 2BASE-TL (-O only) all other values are reserved	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.12.1 PMA/PMD link control (1.30.15)

The STA may enable the PMA/PMD link and initiate link initialization by writing this bit to a one. While link is initializing or up, this bit shall remain a one and writing a one to this bit shall be ignored. The STA may force the link down by writing a zero to this bit. While this bit is set to zero, the PHY shall not send G.994.1 handshake tones. For -O subtypes, upon link drop or MMD reset, the PMA/PMD shall set these bits to zero. For -R subtypes, upon link drop or MMD reset, the PMA/PMD shall set these bits to one.

45.2.1.12.2 STFU (1.30.14)

When this bit is set to a one, the PMA/PMD sends a message to the link partner instructing it to be silent for the silence time (see 45.2.1.12.3). Writing to this bit is valid only when the PMA/PMD link status bits in the PMA/PMD status register (see 45.2.1.13.4) are set to "link is down (ready)". Writes are otherwise ignored.

This bit clears to zero when the silence command is sent, or upon the execution of an MMD reset.

45.2.1.12.3 Silence time (1.30.13:8)

The value of these bits sets the silence time conveyed in a STFU operation (see 45.2.1.12.2). The silence time is encoded according to the following formula, where x is the decimal value of the bits:

$$\text{time} = 10 \times (x + 1) \text{ seconds} \quad (45–1)$$

45.2.1.12.4 Port subtype select (1.30.7)

This register bit selects the port subtype for PMA/PMD operation. The bit defaults to a supported mode. The PHY shall ignore writes that select an unsupported mode (see 45.2.1.12).

Changing this bit alters the fundamental operation of the PMA/PMD, therefore, writes to change this bit shall be ignored if the link is up or initializing (see 45.2.1.13.4).

45.2.1.12.5 Handshake cleardown (1.30.6)

Setting this bit to a one shall cause the PMA/PMD to issue a G.994.1 cleardown command to the link partner (see 61.4.3). The PMA/PMD shall clear this bit to zero after the cleardown command has been sent or upon MMD reset. If the PMA/PMD link is not in the "link down (ready)" state (see 45.2.1.13.4), writes to this register shall be ignored.

45.2.1.12.6 Ignore incoming handshake (1.30.5)

When set to a one, the PMA/PMD shall not respond to received handshake tones (see 61.4.3). When set to a zero, the PMA/PMD shall respond to received handshake tones normally, according to 61.4.3 and G.994.1. Upon MMD reset, this bit shall be cleared to zero.

45.2.1.12.7 PMA/PMD type selection (1.30.4:0)

The PMA/PMD type of a 10P/2B PHY may be selected using bits 4 through 0. A PHY shall ignore writes to the type selection bits that select PMA/PMD types it has not advertised in the speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable port types are applied consistently across all the MMDs on a particular PHY.

A value of 00010 may be set in -R subtype PMA/PMDs that have both 2BASE-TL and 10PASS-TS capability set in the PMA/PMD speed ability register. The PMA/PMD type of the -R is set upon link initialization by the -O.

Values of 00011 and 00100 may be set in -O subtype PMA/PMDs that have both 2BASE-TL and 10PASS-TS capabilities set in the PMA/PMD speed ability register. These values indicate whether the -R is set to 10PASS-TS or 2BASE-TL respectively. If the -R is not capable of the "preferred" mode, the -R is set to 10PASS-TS or 2BASE-TL respectively.

The selection is advertised during link initialization G.994 handshake.

The PMA/PMD type selection defaults to a supported ability.

45.2.1.13 10P/2B PMA/PMD status register (Register 1.31)

The assignment of bits in the 10P/2B PMA/PMD status register is shown in Table 45–13.

Table 45–13—10P/2B PMA/PMD status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.31.15:5	Data rate	Current operating bit rate of the PMD *n* = the value of the bits Data rate = 64*n* kb/s	RO
1.31.4	CO supported	1 = -O subtype operation supported 0 = -O subtype operation not supported	RO
1.31.3	CPE supported	1 = -R subtype operation supported 0 = -R subtype operation not supported	RO
1.31.2:0	PMA/PMD link status	2 1 0 0 0 0 = link is down (not ready) 1 0 0 = link is down (ready) 0 0 1 = link is initializing 0 1 0 = link is up, 10PASS-TS 0 1 1 = link is up, 2BASE-TL all other values reserved	RO

[a]RO = Read Only

45.2.1.13.1 Data rate (1.31.15:5)

These bits indicate the current bit rate of an operational PMA/PMD link. These bits shall be set to all zeros when the link is down or initializing.

45.2.1.13.2 CO supported (1.31.4)

This bit indicates that the PMA/PMD supports operation as a -O subtype. This bit is set to a one when the capability is supported and zero otherwise. This bit reflects the signal PMA_PMD_type in 61.3.2.1.

45.2.1.13.3 CPE supported (1.31.3)

This bit indicates that the PMA/PMD supports operation as a -R subtype. This bit is set to a one when the capability is supported and zero otherwise. This bit reflects the signal PMA_PMD_type in 61.3.2.1.

45.2.1.13.4 PMA/PMD link status (1.31.2:0)

The overall state of the PMA/PMD link is reflected in bits 2:0. After the PMA/PMD is linked to the remote PHY, the PHY shall set these bits to indicate the PMA/PMD port type that is linked (010 for 10PASS-TS and 011 for 2BASE-TL). The corresponding signal, PMA_received_synchronized, is defined in 61.3.2.1.

While the link is initializing, these bits shall be set to 001.

When read as 000, these bits shall indicate that PMA/PMD link is down and the PMA/PMD is not detecting handshake tones from a link partner. This state is known as “not ready”.

When read as 100, these bits shall indicate that the PMA/PMD link is down and the PMA/PMD is detecting handshake tones from a link partner. This state is known as “ready”.

45.2.1.14 Link partner PMA/PMD control register (Register 1.32)

The 10PASS-TS-O and 2BASE-TL-O PMA/PMDs allow access to certain register values of their link partner via the local MDIO interface. A summary of link partner parameters that may be sent or retrieved is provided in Table 45–14.

Table 45–14—Link partner PMA/PMD registers and PMA/PMD register duals

	Register type	Link partner register	Local register counterpart	
	PHY subtype	-O	-O	-R
Link partner register name		**Address and access type[a]**		
10P/2B link partner RX SNR margin		1.38 RO	1.37 RO	1.37 RO
10P/2B link partner line attenuation		1.40 RO	1.39 RO	1.39 RO
10P/2B link partner line quality thresholds		1.42 R/W	1.41 R/W	n/a
10P link partner FEC correctable errors		1.45 RO	1.43 RO	1.43 RO
10P link partner FEC uncorrectable errors		1.46 RO	1.44 RO	1.44 RO
10P link partner electrical length		1.48 RO	1.47 RO	1.47 RO
2B link partner code violation errors		1.90 RO	1.89 RO	1.89 RO
2B link partner errored seconds		1.92 RO	1.91 RO	1.91 RO
2B link partner severely errored seconds		1.94 RO	1.93 RO	1.93 RO
2B link partner LOSW		1.96 RO	1.95 RO	1.95 RO
2B link partner unavailable seconds		1.98 RO	1.97 RO	1.97 RO
2B link partner state defects register		1.100 RO	1.99 RO	1.99 RO

[a]R/W = Read/Write, RO = read only, n/a = undefined

The Link partner PMA/PMD control register allows the -O STA to control the transmission and retrieval of parameters from its -R link partner.

The -R STA may read values exchanged by the -O STA in the local register counterpart to the link partner register. For example, the -O 10P link partner electrical length register will be populated with the contents of the -R 10P electrical length register upon a successful “Get link partner parameters” command. Similarly, the -R 10P/2B line quality thresholds register will contain the values sent by the -O in the 10P/2B link partner line quality thresholds register, after a successful “Send link partner parameters” command.

The link partner registers listed in Table 45–14 have the same behaviour upon being read or reset as their local register counterparts.

This register is defined for -O port subtypes only.

Bit definitions for the Link partner PMA/PMD control register are found in Table 45–15.

Table 45–15—Link partner PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.32.15	Get link partner parameters	1 = get link partner parameters 0 = operation complete, ready	R/W, SC
1.32.14	Reserved	Value always 0, writes ignored	R/W
1.32.13	Send link partner parameters	1 = send link partner parameters 0 = operation complete, ready	R/W, SC
1.32.12:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.14.1 Get link partner parameters (1.32.15)

When this bit is set to a one, the -O PHY updates its link partner registers shown in Table 45–14 with values from the link partner. While the operation is in progress, the PHY shall keep the bit set as one. If the "Get link partner parameters" operation does not complete within 10 seconds, its result shall be marked as "failed" (see 45.2.1.15) and the operation marked as "complete". After completion of the operation or upon reset, the PHY shall reset the bit to zero. A write to this bit when link is down shall cause the result to be marked as "failed" and the operation marked as "complete".

45.2.1.14.2 Send link partner parameters (1.32.13)

When this bit is set to a one, the -O PHY sends the contents of the 2B link partner line quality thresholds register (see 45.2.1.21) to the link partner. While the operation is in progress, the PHY shall keep the bit set as one. The "Send link partner parameters" operation must complete within 10 seconds, or its result shall be marked as "failed" (see 45.2.1.14) and the operation marked as "complete". After completion of the operation or upon reset, the PHY shall reset the bit to zero. A write to this bit when link is down shall cause the result to be marked as "failed" and the operation marked as "complete".

45.2.1.15 Link partner PMA/PMD status register (Register 1.33)

The Link partner PMA/PMD status register reflects the result of the operations that are performed using the Link Partner PMA/PMD control register (1.32).

This register is defined for -O port subtypes only.

Bit definitions for the Link partner PMA/PMD status register are found in Table 45–16.

Table 45–16—Link Partner PMA/PMD status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.33.15	Reserved	Value always 0, writes ignored	RO
1.33.14	Get link partner result	1 = operation failed 0 = operation successful	RO, LH
1.33.13	Reserved	Value always 0, writes ignored	RO

Table 45–16—Link Partner PMA/PMD status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.33.12	Send link partner result	1 = operation failed 0 = operation successful	RO, LH
1.33.11:0	Reserved	Value always 0, writes ignored	RO

[a]RO = Read Only, LH = Latches High

45.2.1.15.1 Get link partner result (1.33.14)

After a “Get link partner parameters” operation terminates, this bit reflects the result of the operation. If the operation did not complete successfully, the PHY shall set this bit to a one. Upon being read or a reset, the PHY shall set the bit to zero.

The definition of an unsuccessful “Get link partner parameters” operation is unspecified and left to the implementation.

45.2.1.15.2 Send link partner result (1.33.12)

After a “Send link partner parameters” operation terminates, this bit reflects the result of the operation. If the operation did not complete successfully, the PHY shall set this bit to a one. Upon being read or a reset, the PHY resets the bit to zero.

The definition of an unsuccessful “Send link partner parameters” operation is unspecified and left to the implementation.

45.2.1.16 10P/2B PMA/PMD link loss register (Register 1.36)

The 10P/2B PMA/PMD link loss register is a 16 bit counter that contains the number of times the PMA/PMD link is lost. Link is considered lost when the PMA_receive_synchronized signal (see 61.3.2.1) transitions from up to down. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PMA/PMD link loss register is shown in Table 45–17.

Table 45–17—10P/2B PMA/PMD link loss register bit definitions

Bit(s)	Name	Description	R/W[a]
1.36.15:0	Link lost events	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.1.17 10P/2B RX SNR margin register (Register 1.37)

For further information on 2BASE-TL SNR margin, see 63.3. For 10PASS-TS SNR margin, see 62.3.

The bit definitions for the 10P/2B RX SNR margin register are found in Table 45–18.

Table 45–18—10P/2B RX SNR margin register bit definition

Bit(s)	Name	Description	R/W[a]
1.37.15:8	Reserved	Value always 0, writes ignored	R/W
1.37.7:0	RX SNR margin	Value of SNR margin in dB	RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.18 10P/2B link partner RX SNR margin register (Register 1.38)

The 10P/2B link partner RX SNR margin register provides access to the link partner's receive SNR margin. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–18.

45.2.1.19 10P/2B line attenuation register (Register 1.39)

This register reports the line attenuation as measured by the PMA/PMD. For more information, see the reference documents in 63.3 and 62.3.

The bit definitions for the 10P/2B line attenuation register are found in Table 45–19.

Table 45–19—10P/2B line attenuation register bit definitions

Bit(s)	Name	Description	R/W[a]
1.39.15:0	Line attenuation	The value of the line attenuation in dB, as perceived by the local PMD.	RO

[a]RO = Read Only

45.2.1.20 10P/2B link partner line attenuation register (Register 1.40)

The 10P/2B link partner line attenuation register provides access to the link partner's perceived line attenuation margin. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–19.

45.2.1.21 10P/2B line quality thresholds register (Register 1.41)

The 10P/2B line quality thresholds register sets the target environment for the 10PASS-TS/2BASE-TL connection. The line quality is defined by the SNR margin and line attenuation values.

Bit definitions for the 10P/2B line quality threshold register are found in Table 45–20.

Table 45–20— 10P/2B line quality thresholds register bit definition

Bit(s)	Name	Description	R/W[a]
1.41.15:8	Loop attenuation threshold	Attenuation threshold in dB	O: R/W R: RO
1.41.7:4	SNR margin threshold	SNR margin threshold in dB	O: R/W R: RO
1.41.3:0	Reserved	Value always 0, writes ignored	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.21.1 Loop attenuation threshold (1.41.15:8)

These bits set the loop attenuation threshold for 2BASE-TL PMA/PMDs. Writing to these bits on a 10PASS-TS PMA/PMD shall have no effect. The threshold value is in units of dB. For more information on the loop attenuation threshold, see 63.2.2.3.

45.2.1.21.2 SNR margin threshold (1.41.7:4)

These bits set the SNR margin threshold for 10PASS-TS and 2BASE-TL PMA/PMDs. The threshold is expressed in units of dB. For more information of the SNR margin threshold, see 63.2.2.3 for 2BASE-TL and Section 10 of the document referenced in 62.1.3 for 10PASS-TS.

45.2.1.22 2B link partner line quality thresholds register (Register 1.42)

The 2B link partner line quality thresholds register allows the -O STA to set its -R link partner's line quality thresholds. The contents of this register are transmitted to the -R when the STA activates the "Send link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.2).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–20.

45.2.1.23 10P FEC correctable errors counter (Register 1.43)

The 10P FEC correctable errors counter is a 16 bit counter that contains the number of FEC codewords that have been received and corrected. For more information on 10PASS-TS FEC, see 62.2.4.2. These bits shall be reset to all zeros upon execution of the MMD reset and upon being read. The assignment of bits in the 10P FEC correctable error counter is shown in Table 45–21.

Table 45–21—10P FEC correctable errors counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.43.15:0	Correctable codewords [15:0]	The bytes of the counter	RO

[a]RO = Read Only

45.2.1.24 10P FEC uncorrectable errors counter (Register 1.44)

The 10P FEC uncorrectable errors counter is a 16 bit counter that contains the number of FEC codewords that have been received and are uncorrectable. For more information on 10PASS-TS FEC, see 62.2.4.2. These bits shall be reset to all zeros upon execution of the MMD reset and upon being read. The assignment of bits in the 10P FEC uncorrectable error counter is shown in Table 45–22.

Table 45–22—10P FEC uncorrectable errors counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.44.15:0	Uncorrectable codewords [15:0]	The bytes of the counter	RO

[a]RO = Read Only

45.2.1.25 10P link partner FEC correctable errors register (Register 1.45)

The 10P link partner FEC correctable errors register provides the -O STA with a snapshot of the -R link partner's FEC correctable errors counter. Because this register is not a counter, its value will increment only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–21 and 45.2.1.23.

45.2.1.26 10P link partner FEC uncorrectable errors register (Register 1.46)

The 10P link partner FEC uncorrectable errors register provides the -O STA a snapshot of the -R link partner's FEC uncorrectable errors counter. Because this register is not a counter, its value will increment only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–22 and 45.2.1.24.

45.2.1.27 10P electrical length register (Register 1.47)

The bit definitions for the 10P electrical length register are found in Table 45–23.

Table 45–23—10P electrical length register bit definitions

Bit(s)	Name	Description	R/W[a]
1.47.15:0	Electrical length	The electrical length of the medium (in meters), as perceived at the local PMD	RO

[a]RO = Read Only

45.2.1.27.1 Electrical length (1.47.15:0)

After the link is established, these bits contain the measured electrical length (in meters) of the medium as measured by the PMD. If the link is down or the PMD is unable to determine the electrical length, these bits shall be set to all ones (see 62.3.2).

45.2.1.28 10P link partner electrical length register (Register 1.48)

The 10P link partner electrical length register provides access to the link partner's electrical length measurement. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–23 and 45.2.1.27.1.

45.2.1.29 10P PMA/PMD general configuration register (Register 1.49)

The 10P PMA/PMD general configuration register is defined for -O port types only.

The 10P PMA/PMD general configuration register bit definitions are found in Table 45–24.

Table 45–24—10P PMA/PMD general configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.49.15:8	Reserved	Value always 0, writes ignored	R/W
1.49.7:0	TX window length	Transmit window length	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.29.1 TX window length (1.49.7:0)

Bits 7:0 control the PMD transmit window length within the cyclic prefix and suffix in units of number of samples, as defined in 62.3.2.

45.2.1.30 10P PSD configuration register (Register 1.50)

This register is defined for -O port subtypes only.

The 10P PSD configuration register bit definitions may be found in Table 45–25.

45.2.1.30.1 PBO disable (1.50.8)

Setting this bit to a one disables UPBO for performance testing purposes. Refer to 62.3.4.4.

45.2.1.31 10P downstream data rate configuration (Registers 1.51, 1.52)

These registers are defined for -O port subtypes only.

Table 45–25—10P PSD configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.50.15:9	Reserved	Value always 0, writes ignored	R/W
1.50.8	PBO disable	1 = PBO disabled 0 = PBO normal operation	O: R/W R: undefined
1.50.7:0	Reserved	Value always 0, writes ignored	O: R/W R: undefined

[a]R/W = Read/Write

The bit definitions for the 10P downstream data rate configuration registers are found in Table 45–26.

Table 45–26—10P downstream data rate configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.51.15:0	Minimum downstream data rate	Sets the minimum required downstream payload data rate *M* = value of bits Data rate = *M* × 64000 b/s	O: R/W R: undefined
1.52.15:0	Maximum downstream data rate	Sets the maximum downstream payload data rate *M* = value of bits Data rate = *M* × 64000 b/s	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.32 10P downstream Reed-Solomon configuration (Register 1.53)

This register is defined for -O port subtypes only.

The bit definitions for 10P downstream Reed-Solomon configuration are found in Table 45–27.

Table 45–27—10P downstream Reed-Solomon configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.53.15:1	Reserved	Value always 0, writes ignored	O: R/W R: undefined
1.53.0	RS codeword length	1 = codeword length of 144 0 = codeword length of 240	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.32.1 RS codeword length (1.53.0)

This bit selects the Reed-Solomon forward error correction codeword length used in the downstream direction. For more information, see 62.2.4.2.

45.2.1.33 10P upstream data rate configuration (Registers 1.54, 1.55)

These registers are defined for -O port subtypes only.

The bit definitions for 10P upstream data rate configuration are found in Table 45–28.

Table 45–28—10P upstream data rate configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.54.15:0	Minimum upstream data rate	Sets the required upstream payload data rate *M* = value of bits Data rate = *M* × 64000 b/s	O: R/W R: undefined
1.55.15:0	Maximum upstream data rate	Sets the maximum upstream payload data rate *M* = value of bits Data rate = *M* × 64000 b/s	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.34 10P upstream 10P upstream Reed-Solomon configuration register (Register 1.56)

This register is defined for -O port subtypes only.

The bit definitions for the 10P upstream Reed-Solomon configuration are found in Table 45–29.

Table 45–29—10P upstream Reed-Solomon configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.56.15:1	Reserved	Value always 0, writes ignored	O: R/W R: undefined
1.56.0	RS codeword length	1 = codeword length = 144 0 = codeword length = 240	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.34.1 RS codeword length (1.56.0)

This bit selects the Reed-Solomon forward error correction codeword length used in the upstream direction. For more information, see 62.2.4.2.

45.2.1.35 10P tone group registers (Registers 1.57, 1.58)

10PASS-TS operates by modulating 4096 individual tones across the transmission spectrum. Each tone can be assigned a PSD level, desired SNR margin and transmission direction (downstream or upstream). To reduce the complexity of addressing individual tones, tones are addressed by group. The STA sets the lower and upper tones in a group, sets the parameters for that group, and issues a command to activate those parameters for that group. See 62.3.4.7 for details on the mechanism that transfers tone information across the link to and from the -R link partner.

This register allows the STA to specify the range of tones to control. The bit definitions for the 10P tone group register are defined in Table 45–30.

Table 45–30—10P tone group register bit definitions

Bit(s)	Name	Description	R/W[a]
1.57.15:0	Lower tone	The number of the lower frequency tone in the group. Valid when ≤ the Upper tone.	R/W
1.58.15:0	Upper tone	The number of the higher frequency tone in the group. Valid when ≥ the Lower tone.	R/W

[a]R/W = Read/Write

45.2.1.36 10P tone control parameters (Registers 1.59, 1.60, 1.61, 1.62, 1.63)

These registers allow the STA to specify parameters for the tones selected in the 10P tone group registers. These values do not take effect until the corresponding activation commands are issued in the 10P tone control action register. The bit definitions for the 10P tone control parameters are shown in Table 45–31.

These registers are defined for -O port subtypes only.

Table 45–31—10P tone control parameters register bit definitions

Bit(s)	Name	Description	R/W[a]
1.59.15	Tone active	1 = selected tones are active 0 = selected tones are disabled	R/W
1.59.14	Tone direction	1 = selected tones assigned to upstream communication 0 = selected tones assigned to downstream communication	R/W
1.59.13:5	Max SNR margin	Assigns the maximum SNR margin the PMD may achieve *M* = value of bits Max SNR margin = *M*/4 dB	R/W
1.59.4:0	Reserved	Value always 0, writes ignored	R/W
1.60:15:9	Reserved	Value always 0, writes ignored	R/W
1.60.8:0	Target SNR margin	Assigns the target SNR margin for the selected tones *M* = value of bits Target SNR margin = *M*/4 dB	R/W
1.61:15:9	Reserved	Value always 0, writes ignored	R/W
1.61.8:0	Min SNR margin	Assigns the minimum SNR margin for the selected tones *M* = value of bits Min SNR margin = *M*/4 dB	R/W
1.62.15:9	Reserved	Value always 0, writes ignored	R/W
1.62.8:0	PSD level	Assigns a TX PSD level for the selected tones in dBm/Hz *P* = value of bits (2's complement) PSD level = *P*/4 - 100 dBm/Hz	R/W
1.63.15:9	Reserved	Value always 0, writes ignored	R/W
1.63.8:0	USPBO reference	Assigns the level of the USPBO reference at the points represented by the selected tones *P* = value of bits (2's complement) PSD level = *P*/4 - 100 dBm/Hz	R/W

[a]R/W = Read/Write

45.2.1.36.1 Tone active (1.59.15)

These bits are used to control the activity of the selected tones. When the “Change tone activity” command is issued (1.64.4), the selected tones will be either activated or deactivated based on the value set in these bits.

45.2.1.36.2 Tone direction (1.59.14)

These bits are used to control the direction of the selected tones. When the “Change tone direction” command is issued (1.64.3), the selected tones will adopt the direction set in these bits.

45.2.1.36.3 Max SNR margin (1.59.13:5)

These bits control the maximum SNR margin for the selected tones. When the “Change SNR margin” command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to maximum SNR margin. The SNR margin is in units of dB, derived by dividing the value of bits 13:5 by 4.

45.2.1.36.4 Target SNR margin (1.60.8:0)

These bits control the target SNR margin for the selected tones. When the “Change SNR margin” command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to target SNR margin. The SNR margin is in units of dB, derived by dividing the value of bits 13:5 by 4.

45.2.1.36.5 Minimum SNR margin (1.61.8:0)

These bits control the minimum SNR margin for the selected tones. When the “Change SNR margin” command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to minimum SNR margin. The SNR margin is in units of dB, derived by dividing the value of bits 13:5 by 4.

45.2.1.36.6 PSD level (1.62.8:0)

These bits control the transmit PSD level of the selected tones. When the “Change PSD level” command is issued (1.64.1), the PMA/PMD will set the PSD level of the selected tones to according to this formula, where *x* is the value of bits 8:0:

$$power = \frac{x}{4} - 100\frac{\text{dBm}}{\text{Hz}} \tag{45–2}$$

45.2.1.36.7 USPBO reference (1.63.8:0)

These bits control the reference level for the upstream power back-off function of the PMA/PMD. When the “Change USPBO reference PSD” command (1.64.0) is issued, the portion of the USPBO reference curve that corresponds to the selected tones is changed to the value specified by these bits. The USPBO reference level is specified according to this formula, where *x* is the value of bits 8:0:

$$power = \frac{x}{4} - 100\frac{\text{dBm}}{\text{Hz}} \tag{45–3}$$

45.2.1.37 10P tone control action register (Register 1.64)

The operations in this register apply to the tones selected in the 10P tone group registers (1.57, 1.58).

This register is defined for -O port subtypes only.

The bit definitions for the 10P tone control action register are shown in Table 45–32.

Table 45–32—10P tone control action register bit definitions

Bit(s)	Name	Description	R/W[a]
1.64.15:6	Reserved	Value always 0, writes ignored	R/W
1.64.5	Refresh tone status	1 = refresh selected tones for the 10P tone status registers 0 = ready, operation complete	R/W, SC
1.64.4	Change tone activity	1 = activate tone active setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.3	Change tone direction	1 = activate tone direction setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.2	Change SNR margin	1 = activate min, max and target SNR margin settings as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.1	Change PSD level	1 = activate PSD level setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.0	Change UPBO reference PSD	1 = activate UPBO reference PSD settings as in tone control parameter register 0 = ready, operation complete	R/W, SC

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.37.1 Refresh tone status (1.64.5)

When this bit is set to a one, the tone status information from the local and link partner is gathered so that it may be read using the 10P tone status registers (1.65, 1.66, and 1.67). While the tones are being refreshed, this bit shall remain set as one. This bit shall be reset to zero when the refresh operation is over or upon reset.

NOTE—Refreshing a large number of tones may take a long time to complete.

45.2.1.37.2 Change tone activity (1.64.4)

When this bit is set to a one, the selected tones are enabled or disabled according to the assignment in the tone active bit of the 10P tone control parameters register (1.59.15). While the tones are being activated/deactivated, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.37.3 Change tone direction (1.64.3)

When this bit is set to a one, the transmission direction of selected tones is changed according to the assignment in the tone direction bit of the 10P tone control parameters register (1.59.14). While the tones are being assigned, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.37.4 Change SNR margin (1.64.2)

When this bit is set to a one, the SNR margin parameters for the selected tones are loaded according the assignment in the Minimum, Target and Maximum SNR margin bits of the 10P tone control parameters register (1.59.13:5, 1.60.8:0, 1.61.8:0). While the parameters are being loaded, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.37.5 Change PSD level (1.64.1)

When this bit is set to a one, the PSD level for the selected tones is set according to the value in the PSD level bits of the 10P tone control parameters register (1.62.8:0). While the PSD is being set, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.37.6 Change USPBO reference PSD (1.64.0)

When this bit is set to a one, the upstream power back-off reference PSD level for the selected tones is set according to the value in the USPBO PSD reference bits of the 10P tone control parameters register (1.63.8:0). While the reference PSD is being set, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.38 10P tone status registers (Registers 1.65, 1.66, 1.67)

The 10P tone status registers allow the STA to query the status of any individual tone in the link. The values read in the 10P tone status register correspond to the tone whose number is set in the "Lower tone" of the 10P tone group registers (see 45.2.1.35).

The status of some tones is read from the link partner. Because the constant update of these values would be a strain on channel resources, these values are only updated for selected tones when the "Refresh tone table" command is issued in the 10P tone control action register (1.64).

The 10P tone status registers bit definitions are given in Table 45–33.

Table 45–33—10P tone status registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.65.15	Refresh status	1 = tone entry has been refreshed 0 = tone entry has not been refreshed since last read	RO
1.65.14	Active	1 = tone is disabled 0 = tone is active	RO
1.65.13	Direction	1 = tone is assigned to upstream communication 0 = tone is assigned to downstream communication	RO
1.65.12:8	Reserved	Value always 0, writes ignored	RO
1.65.7:0	RX PSD	PSD of the tone at the receiver in dBm/Hz	RO
1.66.15:8	TX PSD	PSD of the tone at the transmitter in dBm/Hz	RO
1.66.7:3	Bit load	The number of bits currently loaded on the tone	RO
1.66.2:0	Reserved	Value always 0, writes ignored	RO
1.67.15:10	Reserved	Value always 0, writes ignored	RO
1.67.9:0	SNR margin	Current SNR margin for the tone *R* = value of bits SNR Margin = *R*/4 dB	RO

[a]RO = Read Only

45.2.1.38.1 Refresh status (1.65.15)

When read as a one, bit 1.65.15 indicates that the values for this tone table have not been read since the last "Refresh tone status" command was issued by the 10P tone control action register (1.64). Upon reading this bit or upon reset, the bit shall be reset to zero.

45.2.1.38.2 Active (1.65.14)

When read as a one, this bit indicates that the selected tone is disabled (i.e., powered off and not carrying data).

45.2.1.38.3 Direction (1.65.13)

When read as a one, this bit indicates that the selected tone is assigned to upstream communication. When read as a zero, the tone is assigned to downstream communication.

45.2.1.38.4 RX PSD (1.65.7:0)

These bits report the PSD of the selected tone as perceived at the receiver in units of dBm/Hz.

45.2.1.38.5 TX PSD (1.66.15:8)

These bits report the PSD of the selected tone as output by the transmitter in units of dBm/Hz.

45.2.1.38.6 Bit load (1.66.7:3)

These bits report the number of bits encoded on the selected tone.

45.2.1.38.7 SNR margin (1.67.9:0)

These bits report the current SNR margin for the selected tone, as perceived by the receiver, in units of dB. The value of the SNR margin is obtained by dividing the decimal value of bits 9:0 by 4.

45.2.1.39 10P outgoing indicator bits status register (Register 1.68)

The 10P outgoing indicator bits status register conveys the current state of the indicator bits being sent to the link partner. (See 62.3.4.7) The bit definitions for the 10P indicator bits status register are shown in Table 45–34.

Table 45–34—10P outgoing indicator bits status register bit definition

Bit(s)	Name	Description	R/W[a]
1.68.15:9	Reserved	Value always 0, writes ignored	RO
1.68.8	LoM	1 = received signal below SNR margin threshold 0 = normal state	RO
1.68.7	lpr	1 = power supply voltage invalid 0 = normal state	RO
1.68.6	po	1 = PMA/PMD is being powered off 0 = normal state	RO
1.68.5	Rdi	1 = severely errored frames have been received 0 = normal state	RO
1.68.4	los	1 = signal power is lower than the threshold 0 = normal state	RO
1.68.3:2	Reserved	Value always 0, writes ignored	RO
1.68.1	fec-s	1 = corrected errors have been detected in the received FEC block of slow data 0 = normal state	RO
1.68.0	be-s	1 = non-corrected errors have been detected in the received block of slow data 0 = normal state	RO

[a]RO = Read Only

NOTE—These bit refer to “slow” data. 10PASS-TS uses the slow data channel as referenced in T1.424. The name is kept here to simplify a comparison between the two documents.

45.2.1.39.1 LoM (1.68.8)

When read as a one, this bit indicates that the PMA/PMD is receiving a signal whose SNR margin is below the set threshold (see 45.2.1.21). The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.2 lpr (1.68.7)

When read as a one, this bit indicates that the PMA/PMD is not receiving sufficient power supply input for proper operation. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.3 po (1.68.6)

When read as a one, this bit indicates that the PMA/PMD has been instructed to power off. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.4 Rdi (1.68.5)

When read as a one, this bit indicates that the PMA/PMD has received PMA/PMD frames containing severe errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.5 los (1.68.4)

When read as a one, this bit indicates that the PMA/PMD is not receiving a valid signal. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.6 fec-s (1.68.1)

When read as a one, this bit indicates that the PMA/PMD is receiving FEC blocks with one or more correctable errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.7 be-s (1.68.0)

When read as a one, this bit indicates that the PMA/PMD is receiving FEC blocks with one or more uncorrectable errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40 10P incoming indicator bits status register (Register 1.69)

The 10P indicator bits status register conveys the current state of the indicator bits being received from the link partner's PMA (see 62.3.4.7). The bit definitions for the 10P incoming indicator bits status register are shown in Table 45–35.

Table 45–35—10P incoming indicator bits status register bit definition

Bit(s)	Name	Description	R/W[a]
1.69.15:9	Reserved	Value always 0, writes ignored	RO
1.69.8	LoM	1 = received signal below SNR margin threshold 0 = normal state	RO
1.69.7	Flpr	1 = power supply voltage invalid 0 = normal state	RO
1.69.6	Fpo	1 = PMA/PMD is being powered off 0 = normal state	RO
1.69.5	Rdi	1 = severely errored frames have been received 0 = normal state	RO
1.69.4	Flos	1 = signal power is lower than the threshold 0 = normal state	RO
1.69.3:2	Reserved	Value always 0	RO
1.69.1	Ffec-s	1 = corrected errors have been detected in the received FEC block of slow data 0 = normal state	RO
1.69.0	Febe-s	1 = non-corrected errors have been detected in the received block of slow data 0 = normal state	RO

[a]RO = Read Only

NOTE —These bit refer to "slow" data. 10PASS-TS uses the slow data channel as referenced in T1.424. The name is kept here to simplify a comparison between the two documents.

45.2.1.40.1 LoM (1.69.8)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving a signal whose SNR margin is below the set threshold (see 45.2.1.21). The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.2 Flpr (1.69.7)

When read as a one, this bit indicates that the link partner PMA/PMD is not receiving sufficient power supply input for proper operation. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.3 Fpo (1.69.6)

When read as a one, this bit indicates that the link partner PMA/PMD has been instructed to power off. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.4 Rdi (1.69.5)

When read as a one, this bit indicates that the link partner PMA/PMD has received PMA/PMD frames containing severe errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.5 Flos (1.69.4)

When read as a one, this bit indicates that the link partner PMA/PMD has is not receiving a valid signal. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.6 Ffec-s (1.69.1)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving FEC blocks with one or more correctable errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.7 Febe-s (1.69.0)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving FEC blocks with one or more uncorrectable errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.41 10P cyclic extension configuration register (Register 1.70)

The 10P cyclic extension configuration register controls the length of the cyclic extension for the 10P PMD. For more information, see 62.3.4.2. The value of the cyclic extension is equal to the decimal value set in bits 15:0. Values of decimal 10, 20 and 40 are valid. Writes to set any other values shall be ignored. Upon reset, the PMD shall set these bits to a decimal value of 20.

The bit definitions for this register are shown in Table 45–36.

Table 45–36—10P cyclic extension configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.70.15:0	Cyclic extension	The value of the cyclic extension	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.42 10P attainable downstream data rate register (Register 1.71)

The 10P attainable downstream data rate register reports the data rate that the -R link partner measures to be the highest data rate for downstream transmission. The data rate is encoded as 1 kb/s times the decimal value of the register bits 15:0. The value of the register bits are not valid until after link is “up” (see 45.2.1.13.4).

The bit definitions for this register are found in Table 45–37.

Table 45–37—10P attainable downstream data rate register bit definitions

Bit(s)	Name	Description	R/W[a]
1.71.15:0	Attainable downstream data rate	Data rate in 1 kb/s increments	RO

[a]RO = Read Only

45.2.1.43 2B general parameter register (Register 1.80)

The 2B general parameter register controls various parameters for the operation of the 2BASE-TL PMA/PMD.

This register is read only for -R ports which may be read so the STA may know the mode selected by the -O port. The selected parameters on the -O are sent to the -R link partner on link initialization. For more information on how these parameters are passed across the physical link using G.994.1 signaling, see 61B.3.2.

The bit definitions for the 2B general parameter register are found in Table 45–38.

Table 45–38— 2B general parameter register bit definition

Bit(s)	Name	Description	R/W[a]
1.80.15	Reserved	Value always 0, writes ignored	R/W
1.80.14:10	PMMS target margin	margin = 14:10 - 10dB	R/W
1.80.9	Line probing control	1 = use line probing 0 = do not use line probing (default)	R/W
1.80.8	Noise environment	1 = current condition 0 = worst case (default)	R/W
1.80.7:2	Reserved	Value always 0, writes ignored	R/W
1.80.1:0	Region	Selects the regional annex to operate under 00 = Annex A 01 = Annex B 10 = Annex C 11 = reserved, writes ignored	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.43.1 PMMS target margin (1.80.14:10)

The PMMS target margin specified in bits 14:10 specifies the noise margin that the PMMS procedure tries to attain. The margin is expressed in dB as the decimal value of bits 14:10 minus 10 dB. The margin specified is measured either against either worst case or current line conditions, based on the value set in bit 1.80.8.

The PMMS margin value is transferred during 2BASE-TL initialization via the worst case PMMS margin bits in Table 61B–57 and Table 61B–43, or the current condition PMMS margin bits in Table 61B–48 and Table 61B–44.

45.2.1.43.2 Line probing control (1.80.9)

When set to a one, this bit tells the PMA/PMD to perform line probing the next time link is initialized. When set to a zero, the PMA/PMD does not use line probing. Line probing causes the PMA/PMD to select probe duration and the link data rate. For more information, see the documents referenced in 63.3.

45.2.1.43.3 Noise environment (1.80.8)

This bit controls the reference noise used during line probing. When set to a one, the noise environment is based on the current line conditions. When set to a zero, the noise environment is based on worst case models. For more information, see the documents referenced in 63.3.

45.2.1.43.4 Region (1.80.1:0)

These bits select the regional annex that is used for the operation of the 2BASE-TL PMA/PMD. These annexes refer to clauses in documents referenced by the 2BASE-TL PMA/PMD specification. These are not annexes in IEEE Std 802.3-2002 or its amendments. For details on each annex, see the document referenced in 63.1.3.

45.2.1.44 2B PMD parameters registers (Registers 1.81 through 1.88)

The 2B PMD parameters registers set the transmission parameters for an individual 2BASE-TL PMA/PMD link. When the link is initialized, these parameters are used by the link partner PMA/PMDs in an attempt to achieve specified settings.

These registers allow one to specify a single fixed data rate or up to four data rate ranges at the -O PMA/PMD. An additional set of four data ranges are found in the 2B extended PMD parameters registers (1.102 through 1.109). Bit descriptions for the 2B extended PMD parameters registers are found in 45.2.1.58. Together these sets allow up to eight data rate ranges to be specified.

If at least one data rate range is specified with different Minimum and Maximum data rates, the link is trained with the highest attainable rate. If line probing is enabled, the highest rate is determined by the result of line probing and the “Data rate step” value is ignored. If line probing is disabled, the minimum and maximum rate, “Data rate step” and “Power” values are used to determine the highest attainable rate.

In the case of a single fixed rate specified (Minimum data rate1 equals Maximum data rate1, Data rate step[1:8] set to zero, Minimum/Maximum data rate[2:8] set to zero), the link is trained at the specified rate.

When multiple ranges are specified, the PMD selects the first attainable range, starting sequentially from the first range.

Since writing to this register does not have an immediate effect, reading this register returns the desired parameters, which are not necessarily the current operating parameters.

For more information on how these parameters are passed across the physical link using G.994.1 signaling (see 61B.3.2).

The bit definitions for the 2B PMD parameters register are found in Table 45–39.

Table 45–39— 2B PMD parameters registers bit definition

Bit(s)	Name	Description	R/W[a]
1.81.15	Reserved	Value always 0, writes ignored	R/W
1.81.14:8	Min data rate1	Min data rate of the first range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.81.7	Reserved	Value always 0, writes ignored	R/W
1.81.6:0	Max data rate1	Max data rate of the first range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.82.15:14	Reserved	Value always 0, writes ignored	R/W
1.82.13:7	Data rate step1	Data rate step of the first range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.82.6:2	Power1	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.82.1:0	Constellation1	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.83.15	Reserved	Value always 0, writes ignored	R/W
1.83.14:8	Min data rate2	Min data rate of the second range *n* = value of the bits, *n* valid 3 to 89 Data Rate =64*n* kb/s	O: R/W R: RO
1.83.7	Reserved	Value always 0, writes ignored	R/W
1.83.6:0	Max data rate2	Max data rate of the second range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.84.15:14	Reserved	Value always 0, writes ignored	R/W
1.84.13:7	Data rate step2	Data rate step of the second range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.84.6:2	Power2	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.84.1:0	Constellation2	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.85.15	Reserved	Value always 0, writes ignored	R/W
1.85.14:8	Min data rate3	Min data rate of the third range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.85.7	Reserved	Value always 0, writes ignored	R/W

Table 45–39— 2B PMD parameters registers bit definition *(continued)*

Bit(s)	Name	Description	R/W[a]
1.85.6:0	Max data rate3	Max data rate of the third range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.86.15:14	Reserved	Value always 0, writes ignored	R/W
1.86.13:7	Data rate step3	Data rate step of the third range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.86.6:2	Power3	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.86.1:0	Constellation3	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.87.15	Reserved	Value always 0, writes ignored	R/W
1.87.14:8	Min data rate4	Min data rate of the fourth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.87.7	Reserved	Value always 0, writes ignored	R/W
1.87.6:0	Max data rate4	Max data rate of the fourth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.88.15:14	Reserved	Value always 0, writes ignored	R/W
1.88.13:7	Data rate step4	Data rate step of the fourth range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.88.6:2	Power4	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.88.1:0	Constellation4	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.44.1 Minimum data rate (1.81, 1.83, 1.85, 1.87. Bits 14:8)

Bits 14:8 in registers 1.81 through 1.87 set the minimum data rate for each of the four ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 14:8 by 64.

45.2.1.44.2 Max data rate (1.81, 1.83, 1.85, 1.87. Bits 6:0)

Bits 6:0 in registers 1.81 through 1.87 set the maximum data rate for each of the four ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 6:0 by 64.

45.2.1.44.3 Data rate step (1.82, 1.84, 1.86, 1.88. Bits 13:7)

Bits 13:7 in registers 1.82 through 1.88 set the granularity used by the PMA/PMD when determining the line rate. Valid values for these bits are decimal 1 through 86, writes to set an invalid value shall be ignored. The data rate step is expressed in units of kb/s and is derived by multiplying the decimal value of bits 13:7 by 64.

45.2.1.44.4 Power (1.82, 1.84, 1.86, 1.88. Bits 6:2)

Bits 6:2 in registers 1.82 through 1.88 set the allowed power level for each data rate range. The power levels set in these bits override those of the annex selected in the 2B general parameter register (1.80). The power level is expressed in units of dBm and is derived by the following equation, where *x* equals the value of bits 6:2.

$$power = \left(5 + \frac{x}{2}\right) \text{ dBm} \qquad (45\text{–}4)$$

45.2.1.44.5 Constellation (1.82, 1.84, 1.86, 1.88. Bits 1:0)

Bits 1:0 in registers 1.82 through 1.88 set the allowed constellation for each data rate range. Setting a value of 10 or 01 restricts the constellation to 16- or 32-TCPAM respectively. When set to a value of 00, the PMD automatically determines the constellation during initialization. Attempts to set a value of 11 shall be ignored.

45.2.1.45 2B code violation errors counter (Register 1.89)

The 2B code violation errors counter is a 16-bit counter that contains the number of the 2BASE-TL CRC anomalies. See 63.2.2.3 for more information. These bits shall be set to all zeros upon an MMD reset and upon being read.

Bit definitions for the 2B code violation errors counter are found in Table 45–40.

Table 45–40—2B code violation errors counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.89.15:0	Code violations [15:0]	The bytes of the counter	RO

[a]RO = Read Only

45.2.1.46 2B link partner code violations register (Register 1.90)

The 2B link partner code violations register provides the -O STA with a snapshot of the -R link partner's 2B code violations counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–40.

45.2.1.47 2B errored seconds counter (Register 1.91)

This 8-bit counter contains the number of errored seconds (see 63.2.2.3) These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B errored seconds counter are found in Table 45–41.

Table 45–41—2B errored seconds counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.91.15:8	Reserved	Value always 0, writes ignored	RO
1.91.7:0	Errored seconds [7:0]	The byte of the counter	RO

[a]RO = Read Only

45.2.1.48 2B link partner errored seconds register (Register 1.92)

The 2B link partner errored seconds register provides the -O STA with a snapshot of the -R link partner's 2B errored seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–41.

45.2.1.49 2B severely errored seconds counter (Register 1.93)

This 8-bit counter contains the number severely errored seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B severely errored seconds register are found in Table 45–42.

Table 45–42—2B severely errored counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.93.15:8	Reserved	Value always 0, writes ignored	RO
1.93.7:0	Severely errored seconds [7:0]	The byte of the counter	RO

[a]RO = Read Only

45.2.1.50 2B link partner severely errored seconds register (Register 1.94)

The 2B link partner severely errored seconds register provides the -O STA with a snapshot of the -R link partner's 2B severely errored seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–42.

45.2.1.51 2B LOSW counter (Register 1.95)

This 8-bit counter contains the number of loss of sync seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B LOSW counter are found in Table 45–43.

Table 45–43—2B LOSW counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.95.15:8	Reserved	Value always 0, writes ignored	RO
1.95.7:0	loss of sync seconds [7:0]	The byte of the counter	RO

[a]RO = Read Only

45.2.1.52 2B link partner LOSW register (Register 1.96)

The 2B link partner LOSW register provides the -O STA with a snapshot of the -R link partner's 2B LOSW counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–43.

45.2.1.53 2B unavailable seconds counter (Register 1.97)

This 8-bit counter contains the number of unavailable seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B unavailable seconds counter are found in Table 45–44.

Table 45–44—2B unavailable seconds counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.97.15:8	Reserved	Value always 0, writes ignored	RO
1.97.7:0	unavailable seconds [7:0]	The byte of the counter	RO

[a]RO = Read Only

45.2.1.54 2B link partner unavailable seconds register (Register 1.98)

The 2B link partner unavailable seconds register provides the -O STA with a snapshot of the -R link partner's 2B unavailable seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–44.

45.2.1.55 2B state defects register (Register 1.99)

The 2B state defects register is used to communicate defect states from the 2BASE-TL PMD (see 63.2.2.3). The thresholds for these defects are set using the 2B line quality threshold register (see 45.2.1.21). The register bits are cleared to zero when read by the STA or upon MMD reset. On a -R PMA/PMD, these bits are also cleared to zero upon the successful reception of a "Get link partner parameters" command (see 45.2.1.13.1).

Bit definitions for the 2B state defects register are found in Table 45–45.

Table 45–45—2B state defects register bit definitions

Bit(s)	Name	Description	R/W[a]
1.99.15	Segment defect	1 = segment defect detected 0 = normal condition	RO, LH
1.99.14	SNR margin defect	1 = SNR margin defect detected 0 = normal condition	RO, LH
1.99.13	Loop attenuation defect	1 = loop attenuation defect detected 0 = normal condition	RO, LH
1.99.12	Loss of sync word	1 = loss of sync word detected 0 = normal condition	RO, LH
1.99.11:0	Reserved	Value always 0, writes ignored	R/W

[a]RO = Read Only, LH = Latching High, R/W = Read/Write

45.2.1.55.1 Segment defect (1.99.15)

When read as a one, this bit indicates that the local PMA/PMD has detected a segment defect.

45.2.1.55.2 SNR margin defect (1.99.14)

When read as a one, this bit indicates that the local PMA/PMD has received a signal whose SNR is below the set threshold (see 45.2.1.21).

45.2.1.55.3 Loop attenuation defect (1.99.13)

When read as a one, this bit indicates that the PMA/PMD has detected that the loop attenuation is below the set threshold (see 45.2.1.21).

45.2.1.55.4 Loss of sync word (1.99.12)

When read as a one, this bit indicates that the PMA/PMD has lost PMA/PMD frame sync.

45.2.1.56 2B link partner state defects register (Register 1.100)

The 2B link partner state defects register provides the -O STA with a snapshot of the -R link partner's 2B state defects register. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.14) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–45.

45.2.1.57 2B negotiated constellation register (Register 1.101)

The bit definitions for this register are shown in Table 45–46.

Table 45–46—2B register bit definition

Bit(s)	Name	Description	R/W[a]
1.101.15:2	Reserved	Value always 0, writes ignored	R/W
1.101.1:0	Negotiated constellation	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = undetermined	RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.57.1 Negotiated constellation (1.101.1:0)

These bits report the resulting constellation that was obtained after initialization. For more information on configuring 2BASE-TL PMA/PMD link initialization, see the 2B PMD parameter registers (see 45.2.1.44). When read as 10 or 01, the constellation has been set as either 16- or 32-TCPAM respectively. When read as 00, the local PMD has not arrived at a constellation with its link partner (as may be the case while link is down or initializing, after reset or upon a failed initialization).

45.2.1.58 2B extended PMD parameters registers (Registers 1.102 through 1.109)

The 2B extended PMD parameters registers define four additional data range sets to be used in conjunction with the 2B PMD parameters registers when additional PMD configuration detail is desired. For a complete description of the use of these registers, see 45.2.1.44.

Bit definitions for these registers can be found in Table 45–47

Table 45–47— 2B extended PMD parameters registers bit definition

Bit(s)	Name	Description	R/W[a]
1.102.15	Reserved	Value always 0, writes ignored	R/W
1.102.14:8	Min data rate5	Min data rate of the fifth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.102.7	Reserved	Value always 0, writes ignored	R/W
1.102.6:0	Max data rate5	Max data rate of the fifth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.103.15:14	Reserved	Value always 0, writes ignored	R/W
1.103.13:7	Data rate step5	Data rate step of the fifth range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.103.6:2	Power5	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.103.1:0	Constellation5	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.104.15	Reserved	Value always 0, writes ignored	R/W
1.104.14:8	Min data rate6	Min data rate of the sixth range *n* = value of the bits, *n* valid 3 to 89 Data Rate =64*n* kb/s	O: R/W R: RO
1.104.7	Reserved	Value always 0, writes ignored	R/W
1.104.6:0	Max data rate6	Max data rate of the sixth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.105.15:14	Reserved	Value always 0, writes ignored	R/W
1.105.13:7	Data rate step6	Data rate step of the sixth range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.105.6:2	Power6	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.105.1:0	Constellation6	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.106.15	Reserved	Value always 0, writes ignored	R/W
1.106.14:8	Min data rate7	Min data rate of the seventh range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.106.7	Reserved	Value always 0, writes ignored	R/W

Table 45–47— 2B extended PMD parameters registers bit definition *(continued)*

Bit(s)	Name	Description	R/W[a]
1.106.6:0	Max data rate7	Max data rate of the seventh range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.107.15:14	Reserved	Value always 0, writes ignored	R/W
1.107.13:7	Data rate step7	Data rate step of the seventh range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.107.6:2	Power7	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.107.1:0	Constellation7	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.108.15	Reserved	Value always 0, writes ignored	R/W
1.108.14:8	Min data rate8	Min data rate of the eighth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.108.7	Reserved	Value always 0, writes ignored	R/W
1.108.6:0	Max data rate8	Max data rate of the eighth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.109.15:14	Reserved	Value always 0, writes ignored	R/W
1.109.13:7	Data rate step8	Data rate step of the eighth range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.109.6:2	Power8	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.109.1:0	Constellation8	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.58.1 Minimum data rate (1.102, 1.104, 1.106, 1.108. Bits 14:8)

Bits 14:8 in registers 1.102, 1.104, 1.106, and 1.108 set the minimum data rate for each of the four extended ranges. Valid values for these bits are decimal 3 through 89. writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 14:8 by 64.

45.2.1.58.2 Max data rate (1.102, 1.104, 1.106, 1.108. Bits 6:0)

Bits 6:0 in registers 1.102, 1.104, 1.106, and 1.108 set the maximum data rate for each of the four extended ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 6:0 by 64.

45.2.1.58.3 Data rate step (1.103, 1.105, 1.107, 1.109. Bits 13:7)

Bits 13:7 in registers 1.103, 1.105, 1.107 and 1.109 set the granularity used by the PMA/PMD when determining the line rate. Valid values for these bits are decimal 1 through 86, writes to set an invalid value shall be ignored. The data rate step is expressed in units of kb/s and is derived by multiplying the decimal value of bits 13:7 by 64.

45.2.1.58.4 Power (1.103, 1.105, 1.107, 1.109. Bits 6:2)

Bits 6:2 in registers 1.103, 1.105, 1.107 and 1.109 set the allowed power level for each extended data rate range. The power levels set in these bits override those of the annex selected in the 2B general parameter register (1.80). The power level is expressed in units of dBm and is derived by the following equation, where *x* equals the value of bits 6:2.

$$\text{power} = \left(5 + \frac{x}{2}\right) \text{ dBm} \tag{45–5}$$

45.2.1.58.5 Constellation (1.103, 1.105, 1.107, 1.109. Bits 1:0)

Bits 1:0 in registers 1.103, 1.105, 1.107 and 1.109 set the allowed constellation for each extended data rate range. Setting a value of 10 or 01 restricts the constellation to 16- or 32-TCPAM respectively. When set to a value of 00, the PMD automatically determines the constellation during initialization. Attempts to set a value of 11 shall be ignored.

45.2.2 WIS registers

The assignment of registers in the WIS is shown in Table 45–48. For the WIS octet fields, bit 8 of the corresponding field in the WIS frame maps to the lowest numbered bit of the field in the register.

Table 45–48—WIS registers

Register address	Register name
2.0	WIS control 1
2.1	WIS status 1
2.2, 2.3	WIS device identifier
2.4	WIS speed ability
2.5, 2.6	WIS devices in package
2.7	10G WIS control 2
2.8	10G WIS status 2
2.9	10G WIS test-pattern error counter
2.10 through 2.13	Reserved
2.14, 2.15	WIS package identifier
2.16 through 2.32	Reserved

Table 45–48—WIS registers *(continued)*

Register address	Register name
2.33	10G WIS status 3
2.34 through 2.36	Reserved
2.37	10G WIS far end path block error count
2.38	Reserved
2.39 through 2.46	10G WIS J1 transmit
2.47 through 2.54	10G WIS J1 receive
2.55, 2.56	10G WIS far end line BIP errors
2.57, 2.58	10G WIS line BIP errors
2.59	10G WIS path block error count
2.60	10G WIS section BIP error count
2.61 through 2.63	Reserved
2.64 through 2.71	10G WIS J0 transmit
2.72 through 2.79	10G WIS J0 receive
2.80 through 2.32 767	Reserved
2.32 768 through 2.65 535	Vendor specific

45.2.2.1 WIS control 1 register (Register 2.0)

The assignment of bits in the WIS control 1 register is shown in Table 45–49. The default value for each bit of the WIS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.2.1.1 Reset (2.0.15)

Resetting a WIS is accomplished by setting bit 2.0.15 to a one. This action shall set all WIS registers to their default states. As a consequence, this action may change the internal state of the WIS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a WIS shall return a value of one in bit 2.0.15 when a reset is in progress and a value of zero otherwise. A WIS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 2.0.15. During a reset, a WIS shall respond to reads from register bits 2.0.15 and 2.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

Table 45–49— WIS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.0.15	Reset	1 = WIS reset 0 = Normal operation	R/W SC
2.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
2.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.12	Reserved	Value always 0, writes ignored	R/W
2.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
2.0.10:7	Reserved	Value always 0, writes ignored	R/W
2.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
2.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.2.1.2 Loopback (2.0.14)

The WIS shall be placed in a loopback mode of operation when bit 2.0.14 is set to a one. When bit 2.0.14 is set to a one, the WIS shall ignore all data presented to it by the PMA sublayer. When bit 2.0.14 is set to a one, the WIS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the detailed behavior of the WIS during loopback is specified in 50.3.9

The default value of bit 2.0.14 is zero.

NOTE—The signal path through the WIS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the WIS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.2.1.3 Low power (2.0.11)

A WIS may be placed into a low-power mode by setting bit 2.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the WIS. The behavior of the WIS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 2.0.11 is zero.

45.2.2.1.4 Speed selection (2.0.13, 2.0.6, and 2.0.5:2)

Speed selection bits 2.0.13 and 2.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the WIS may be selected using bits 5 through 2. The speed abilities of the WIS are advertised in the WIS speed ability register. A WIS may ignore writes to the WIS speed selection bits that select speeds it has not advertised in the WIS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The WIS speed selection defaults to a supported ability.

45.2.2.2 WIS status 1 register (Register 2.1)

The assignment of bits in the WIS status 1 register is shown in Table 45–50. All the bits in the WIS status 1 register are read only; a write to the WIS status 1 register shall have no effect.

Table 45–50—WIS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.1.15:8	Reserved	Ignore when read	RO
2.1.7	Fault	1 = Fault condition 0 = No fault condition	RO/LH
2.1.6:3	Reserved	Ignore when read	RO
2.1.2	Link status	1 = WIS link up 0 = WIS link down	RO/LL
2.1.1	Low-power ability	1 = WIS supports low-power mode 0 = WIS does not support low-power mode	RO
2.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High, LL = Latching Low

45.2.2.2.1 Fault (2.1.7)

When read as a one, bit 2.1.7 indicates that the WIS has detected a fault condition. When read as a zero, bit 2.1.7 indicates that the WIS has not detected a fault condition. The fault bit shall be implemented with latching high behavior.

The default value of bit 2.1.7 is zero.

45.2.2.2.2 Link status (2.1.2)

When read as a one, bit 2.1.2 indicates that the WIS receive link is up. When read as a zero, bit 2.1.2 indicates that the WIS receive link is down. The link status bit shall be implemented with latching low behavior.

45.2.2.2.3 Low-power ability (2.1.1)

When read as a one, bit 2.1.1 indicates that the WIS supports the low-power feature. When read as a zero, bit 2.1.1 indicates that the WIS does not support the low-power feature. If a WIS supports the low-power feature, then it is controlled using the low-power bit in the WIS control register.

45.2.2.3 WIS device identifier (Registers 2.2 and 2.3)

Registers 2.2 and 2.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of WIS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS device identifier.

The format of the WIS device identifier is specified in 22.2.4.3.1.

45.2.2.4 WIS speed ability (Register 2.4)

The assignment of bits in the WIS speed ability register is shown in Table 45–51.

Table 45–51— WIS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
2.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
2.4.0	10G capable	1 = WIS is capable of operating at 10 Gb/s 0 = WIS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.2.4.1 10G capable (2.4.0)

When read as a one, bit 2.4.0 indicates that the WIS is able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate). When read as a zero, bit 2.4.0 indicates that the WIS is not able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate).

45.2.2.5 WIS devices in package (Registers 2.5 and 2.6)

The WIS devices in package registers are defined in Table 45–2.

45.2.2.6 10G WIS control 2 register (Register 2.7)

The assignment of bits in the 10G WIS control 2 register is shown in Table 45–52. The default value for each bit of the 10G WIS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.2.6.1 PRBS31 receive test-pattern enable (2.7.5)

If the WIS supports the optional PRBS31 (see 49.2.8) pattern testing advertised in bit 2.8.1 and the mandatory receive test-pattern enable bit (2.7.2) is not one, setting bit 2.7.5 to a one shall set the receive path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.5 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2.

Table 45–52—10G WIS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.7.15:6	Reserved	Value always 0, writes ignored	R/W
2.7.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
2.7.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
2.7.3	Test-pattern selection	1 = Select square wave test pattern 0 = Select mixed-frequency test pattern	R/W
2.7.2	Receive test-pattern enable	1 = Enable test-pattern mode on the receive path 0 = Disable test-pattern mode on the receive path	R/W
2.7.1	Transmit test-pattern enable	1 = Enable test-pattern mode on the transmit path 0 = Disable test-pattern mode on the transmit path	R/W
2.7.0	PCS type selection	1 = Select 10GBASE-W PCS type 0 = Select 10GBASE-R PCS type	R/W

[a]R/W = Read/Write

45.2.2.6.2 PRBS31 transmit test-pattern enable (2.7.4)

If the WIS supports the optional PRBS31 pattern testing advertised in bit 2.8.1 and the mandatory transmit test-pattern enable bit (2.7.1) is not one, then setting bit 2.7.4 to a one shall set the transmit path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2.

45.2.2.6.3 Test-pattern selection (2.7.3)

Bit 2.7.3 controls the type of pattern sent by the transmitter when in test-pattern mode. Setting bit 2.7.3 to a one shall select the square wave test pattern. Setting bit 2.7.3 to a zero shall select the mixed-frequency test pattern. The details of the test patterns are specified in Clause 50

45.2.2.6.4 Receive test-pattern enable (2.7.2)

Setting bit 2.7.2 to a one shall set the receive path of the WIS into the test-pattern mode. Setting bit 2.7.2 to a zero shall disable the test-pattern mode on the receive path of the WIS. The behavior of the WIS when in test-pattern mode is specified in Clause 50

45.2.2.6.5 Transmit test-pattern enable (2.7.1)

Setting bit 2.7.1 to a one shall set the transmit path of the WIS into the test-pattern mode. Setting bit 2.7.1 to a zero shall disable the test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in test-pattern mode is specified in Clause 50

45.2.2.6.6 PCS type selection (2.7.0)

Setting bit 2.7.0 to a one shall enable the 10GBASE-W logic and set the speed of the WIS-PMA interface to 9.95328 Gb/s. Setting bit 2.7.0 to a zero shall disable the 10GBASE-W logic, set the speed of the PCS-PMA interface to 10.3125 Gb/s and bypass the data around the 10GBASE-W logic. A WIS that is only capable of

supporting 10GBASE-W operation and is unable to support 10GBASE-R operation shall ignore values written to this bit and shall return a value of one when read. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

45.2.2.7 10G WIS status 2 register (Register 2.8)

The assignment of bits in the 10G WIS status 2 register is shown in Table 45–53. All the bits in the 10G WIS status 2 register are read only; a write to the 10G WIS status 2 register shall have no effect.

Table 45–53—10G WIS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
2.8.13:2	Reserved	Ignore when read	RO
2.8.1	PRBS31 pattern testing ability	1 = WIS is able to support PRBS31 pattern testing 0 = WIS is not able to support PRBS31 pattern testing	RO
2.8.0	10GBASE-R ability	1 = WIS is able to support 10GBASE-R port types 0 = WIS is not able to support 10GBASE-R port types	RO

[a]RO = Read Only

45.2.2.7.1 Device present (2.8.15:14)

When read as <10>, bits 2.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 2.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

45.2.2.7.2 PRBS31 pattern testing ability (2.8.1)

When read as a one, bit 2.8.1 indicates that the WIS is able to support PRBS31 pattern testing. When read as a zero, bit 2.8.1 indicates that the WIS is not able to support PRBS31 pattern testing. If the WIS is able to support PRBS31 pattern testing, then the pattern generation and checking is controlled using bits 2.7.5:4.

45.2.2.7.3 10GBASE-R ability (2.8.0)

When read as a one, bit 2.8.0 indicates that the WIS is able to bypass the WIS logic and adjust the XSBI interface speed to support 10GBASE-R port types. When read as a zero, bit 2.8.0 indicates that the WIS is not able to bypass the WIS logic and cannot support 10GBASE-R port types.

45.2.2.8 10G WIS test-pattern error counter register (Register 2.9)

The assignment of bits in the 10G WIS test-pattern error counter register is shown in Table 45–54. This register is only required when the PRBS31 pattern generation capability is supported.

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the

Table 45–54—10G WIS test-pattern error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
2.9.15:0	Test-pattern error counter	Error counter	RO

[a]RO = Read Only

management function or upon execution of the WIS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.8.

45.2.2.9 WIS package identifier (Registers 2.14 and 2.15)

Registers 2.14 and 2.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the WIS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the WIS package identifier is specified in 22.2.4.3.1.

45.2.2.10 10G WIS status 3 register (Register 2.33)

The assignment of bits in the 10G WIS status 3 register is shown in Table 45–55. All the bits in the 10G WIS status 3 register are read only; a write to the 10G WIS status 3 register shall have no effect.

Table 45–55—10G WIS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.33.15:12	Reserved	Ignore when read	RO
2.33.11	SEF	Severely errored frame	RO/LH
2.33.10	Far end PLM-P/LCD-P	1 = Far end path label mismatch / Loss of code-group delineation 0 = No far end path label mismatch / Loss of code-group delineation	RO/LH
2.33.9	Far end AIS-P/LOP-P	1 = Far end path alarm indication signal / Path loss of pointer 0 = No far end path alarm indication signal / Path loss of pointer	RO/LH
2.33.8	Reserved	Ignore when read	RO
2.33.7	LOF	1 = Loss of frame flag raised 0 = Loss of frame flag lowered	RO/LH
2.33.6	LOS	1 = Loss of signal flag raised 0 = Loss of signal flag lowered	RO/LH

Table 45–55—10G WIS status 3 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
2.33.5	RDI-L	1 = Line remote defect flag raised 0 = Line remote defect flag lowered	RO/LH
2.33.4	AIS-L	1 = Line alarm indication flag raised 0 = Line alarm indication flag lowered	RO/LH
2.33.3	LCD-P	1 = Path loss of code-group delineation flag raised 0 = Path loss of code-group delineation flag lowered	RO/LH
2.33.2	PLM-P	1 = Path label mismatch flag raised 0 = Path label mismatch flag lowered	RO/LH
2.33.1	AIS-P	1 = Path alarm indication signal raised 0 = Path alarm indication signal lowered	RO/LH
2.33.0	LOP-P	1 = Loss of pointer flag raised 0 = Loss of pointer flag lowered	RO/LH

[a]RO = Read Only, LH = Latching High

45.2.2.10.1 SEF (2.33.11)

When read as a one, bit 2.33.11 indicates that the SEF flag has been raised by the WIS. When read as a zero, bit 2.33.11 indicates that the SEF flag is lowered. The SEF bit shall be implemented with latching high behavior.

The SEF functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.2 Far end PLM-P/LCD-P (2.33.10)

When read as a one, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag is lowered. The far end PLM-P/LCD-P bit shall be implemented with latching high behavior.

The far end path label mismatch/loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.3 Far end AIS-P/LOP-P (2.33.9)

When read as a one, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag has been raised by the WIS. When read as a zero, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag is lowered. The far end AIS-P/LOP-P bit shall be implemented with latching high behavior.

The far end path alarm indication signal/path loss of pointer functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.4 LOF (2.33.7)

When read as a one, bit 2.33.7 indicates that the loss of frame flag has been raised. When read as a zero, bit 2.33.7 indicates that the loss of frame flag is lowered. The LOF bit shall be implemented with latching high behavior.

The LOF functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.5 LOS (2.33.6)

When read as a one, bit 2.33.6 indicates that the loss of signal flag has been raised. When read as a zero, bit 2.33.6 indicates that the loss of signal flag is lowered. The LOS bit shall be implemented with latching high behavior.

The LOS functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.6 RDI-L (2.33.5)

When read as a one, bit 2.33.5 indicates that the line remote defect flag has been raised. When read as a zero, bit 2.33.5 indicates that the line remote defect flag is lowered. The RDI-L bit shall be implemented with latching high behavior.

The RDI-L functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.7 AIS-L (2.33.4)

When read as a one, bit 2.33.4 indicates that the line alarm indication flag has been raised. When read as a zero, bit 2.33.4 indicates that the line alarm indication flag is lowered. The AIS-L bit shall be implemented with latching high behavior.

The AIS-L functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.8 LCD-P (2.33.3)

When read as a one, bit 2.33.3 indicates that the loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.3 indicates that the loss of code-group delineation flag is lowered. The LCD-P bit shall be implemented with latching high behavior.

The loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.9 PLM-P (2.33.2)

When read as a one, bit 2.33.2 indicates that the path label mismatch flag has been raised. When read as a zero, bit 2.33.2 indicates that the path label mismatch flag is lowered. The PLM-P bit shall be implemented with latching high behavior.

The PLM-P functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.10 AIS-P (2.33.1)

When read as a one, bit 2.33.1 indicates that the path alarm indication signal has been raised. When read as a zero, bit 2.33.1 indicates that the path alarm indication signal is lowered. The AIS-P bit shall be implemented with latching high behavior.

The path alarm indication signal functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.11 LOP-P (2.33.0)

When read as a one, bit 2.33.0 indicates that the loss of pointer flag has been raised. When read as a zero, bit 2.33.0 indicates that the loss of pointer flag is lowered. The LOP-P bit shall be implemented with latching high behavior.

The LOP-P functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.11 10G WIS far end path block error count (Register 2.37)

The assignment of bits in the 10G WIS far end path block error count register is shown in Table 45–56.

Table 45–56—10G WIS far end path block error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.37.15:0	Far end path block error count	Far end path block error count	RO

[a]RO = Read Only,

The 10G WIS far end path block error count is incremented by one whenever a far end path block error, defined in Annex 50A, is detected as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.12 10G WIS J1 transmit (Registers 2.39 through 2.46)

The assignment of octets in the 10G WIS J1 transmit registers is shown in Table 45–57.

Table 45–57—10G WIS J1 transmit 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.46.15:8	J1 transmit 15	Transmitted path trace octet 15	R/W
2.46.7:0	J1 transmit 14	Transmitted path trace octet 14	R/W
2.45.15:8	J1 transmit 13	Transmitted path trace octet 13	R/W
2.45.7:0	J1 transmit 12	Transmitted path trace octet 12	R/W
2.44.15:8	J1 transmit 11	Transmitted path trace octet 11	R/W
2.44.7:0	J1 transmit 10	Transmitted path trace octet 10	R/W
2.43.15:8	J1 transmit 9	Transmitted path trace octet 9	R/W
2.43.7:0	J1 transmit 8	Transmitted path trace octet 8	R/W
2.42.15:8	J1 transmit 7	Transmitted path trace octet 7	R/W

Table 45–57—10G WIS J1 transmit 0–15 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
2.42.7:0	J1 transmit 6	Transmitted path trace octet 6	R/W
2.41.15:8	J1 transmit 5	Transmitted path trace octet 5	R/W
2.41.7:0	J1 transmit 4	Transmitted path trace octet 4	R/W
2.40.15:8	J1 transmit 3	Transmitted path trace octet 3	R/W
2.40.7:0	J1 transmit 2	Transmitted path trace octet 2	R/W
2.39.15:8	J1 transmit 1	Transmitted path trace octet 1	R/W
2.39.7:0	J1 transmit 0	Transmitted path trace octet 0	R/W

[a]R/W = Read/Write

The first transmitted path trace octet is J1 transmit 15, which contains the delineation octet. The default value for the J1 transmit 15 octet is 137 (hexadecimal 89). The last transmitted path trace octet is J1 transmit 0. The default value for the J1 transmit 0 through 14 octets is 0. The transmitted path trace is described in 50.3.2.1.

45.2.2.13 10G WIS J1 receive (Registers 2.47 through 2.54)

The assignment of octets in the 10G WIS J1 receive registers is shown in Table 45–58.

Table 45–58—10G WIS J1 receive 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.54.15:8	J1 receive 15	Received path trace octet 15	RO
2.54.7:0	J1 receive 14	Received path trace octet 14	RO
2.53.15:8	J1 receive 13	Received path trace octet 13	RO
2.53.7:0	J1 receive 12	Received path trace octet 12	RO
2.52.15:8	J1 receive 11	Received path trace octet 11	RO
2.52.7:0	J1 receive 10	Received path trace octet 10	RO
2.51.15:8	J1 receive 9	Received path trace octet 9	RO
2.51.7:0	J1 receive 8	Received path trace octet 8	RO
2.50.15:8	J1 receive 7	Received path trace octet 7	RO
2.50.7:0	J1 receive 6	Received path trace octet 6	RO
2.49.15:8	J1 receive 5	Received path trace octet 5	RO

Table 45–58—10G WIS J1 receive 0–15 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
2.49.7:0	J1 receive 4	Received path trace octet 4	RO
2.48.15:8	J1 receive 3	Received path trace octet 3	RO
2.48.7:0	J1 receive 2	Received path trace octet 2	RO
2.47.15:8	J1 receive 1	Received path trace octet 1	RO
2.47.7:0	J1 receive 0	Received path trace octet 0	RO

[a]RO = Read Only

The first received path trace octet is J1 receive 15. The last received path trace octet is J1 receive 0. The received path trace is described in 50.3.2.4.

45.2.2.14 10G WIS far end line BIP errors (Registers 2.55 and 2.56)

The assignment of octets in the 10G WIS far end line BIP errors registers is shown in Table 45–59.

Table 45–59—10G WIS far end line BIP errors 0–1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.56.15:0	WIS far end line BIP errors 0	Least significant word of the WIS far end line BIP errors counter	RO
2.55.15:0	WIS far end line BIP errors 1	Most significant word of the WIS far end line BIP errors counter	RO

[a]RO = Read Only

The 10G WIS far end line BIP Errors register pair reflects the contents of the far end line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of far end line BIP errors reported by the far end, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.55) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.55 and the least significant 16 bits appearing in 2.56, the value being latched before the contents of 2.55 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.56 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

NOTE—These counters do not follow the behaviour described in 45.2 for 32-bit counters.

45.2.2.15 10G WIS line BIP errors (Registers 2.57 and 2.58)

The assignment of octets in the 10G WIS line BIP errors registers is shown in Table 45–60.

The 10G WIS line BIP errors register pair reflects the contents of the line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of line BIP errors detected on the incoming

Table 45–60—10G WIS line BIP errors 0–1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.58.15:0	WIS line BIP errors 0	Least significant word of the WIS line BIP errors counter	RO
2.57.15:0	WIS line BIP errors 1	Most significant word of the WIS line BIP errors counter	RO

[a]RO = Read Only

data stream, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.57) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.57 and the least significant 16 bits appearing in 2.58, the value being latched before the contents of 2.57 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.58 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

NOTE—These counters do not follow the behaviour described in 45.2 for 32-bit counters.

45.2.2.16 10G WIS path block error count (Register 2.59)

The assignment of bits in the 10G WIS path block error count register is shown in Table 45–61.

Table 45–61—10G WIS path block error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.59.15:0	Path block error count	Path block error counter	RO

[a]RO = Read Only

45.2.2.16.1 Path block error count (2.59.15:0)

The path block error count is incremented by one whenever a B3 parity error (defined in Annex 50A) is detected, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.17 10G WIS section BIP error count (Register 2.60)

The assignment of bits in the 10G WIS section BIP error count register is shown in Table 45–62.

Table 45–62—10G WIS section BIP error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.60.15:0	Section BIP error count	Section BIP error count	RO

[a]RO = Read Only

45.2.2.17.1 Section BIP error count (2.60.15:0)

The section BIP error count is incremented by the number of section BIP errors detected within each WIS frame, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.18 10G WIS J0 transmit (Registers 2.64 through 2.71)

The assignment of octets in the 10G WIS J0 transmit registers is shown in Table 45–63.

Table 45–63—10G WIS J0 transmit 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.71.15:8	J0 transmit 15	Transmitted section trace octet 15	R/W
2.71.7:0	J0 transmit 14	Transmitted section trace octet 14	R/W
2.70.15:8	J0 transmit 13	Transmitted section trace octet 13	R/W
2.70.7:0	J0 transmit 12	Transmitted section trace octet 12	R/W
2.69.15:8	J0 transmit 11	Transmitted section trace octet 11	R/W
2.69.7:0	J0 transmit 10	Transmitted section trace octet 10	R/W
2.68.15:8	J0 transmit 9	Transmitted section trace octet 9	R/W
2.68.7:0	J0 transmit 8	Transmitted section trace octet 8	R/W
2.67.15:8	J0 transmit 7	Transmitted section trace octet 7	R/W
2.67.7:0	J0 transmit 6	Transmitted section trace octet 6	R/W
2.66.15:8	J0 transmit 5	Transmitted section trace octet 5	R/W
2.66.7:0	J0 transmit 4	Transmitted section trace octet 4	R/W
2.65.15:8	J0 transmit 3	Transmitted section trace octet 3	R/W
2.65.7:0	J0 transmit 2	Transmitted section trace octet 2	R/W
2.64.15:8	J0 transmit 1	Transmitted section trace octet 1	R/W
2.64.7:0	J0 transmit 0	Transmitted section trace octet 0	R/W

[a]R/W = Read/Write

The J0 transmit octets allow a receiver to verify its continued connection to the WIS transmitter. The first transmitted section trace octet is J0 transmit 15, which contains the delineation octet. The default value for the J0 transmit 15 octet is 137 (hexadecimal 89). The last transmitted section trace octet is J0 transmit 0. The default value for the J0 transmit 0 through 14 octets is 0. The transmitted section trace is described in 50.3.2.3.

45.2.2.19 10G WIS J0 receive (Registers 2.72 through 2.79)

The assignment of octets in the 10G WIS J0 receive registers is shown in Table 45–64.

Table 45–64— 10G WIS J0 receive 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.79.15:8	J0 receive 15	Received section trace octet 15	RO
2.79.7:0	J0 receive 14	Received section trace octet 14	RO
2.78.15:8	J0 receive 13	Received section trace octet 13	RO
2.78.7:0	J0 receive 12	Received section trace octet 12	RO
2.77.15:8	J0 receive 11	Received section trace octet 11	RO
2.77.7:0	J0 receive 10	Received section trace octet 10	RO
2.76.15:8	J0 receive 9	Received section trace octet 9	RO
2.76.7:0	J0 receive 8	Received section trace octet 8	RO
2.75.15:8	J0 receive 7	Received section trace octet 7	RO
2.75.7:0	J0 receive 6	Received section trace octet 6	RO
2.74.15:8	J0 receive 5	Received section trace octet 5	RO
2.74.7:0	J0 receive 4	Received section trace octet 4	RO
2.73.15:8	J0 receive 3	Received section trace octet 3	RO
2.73.7:0	J0 receive 2	Received section trace octet 2	RO
2.72.15:8	J0 receive 1	Received section trace octet 1	RO
2.72.7:0	J0 receive 0	Received section trace octet 0	RO

[a]RO = Read Only

The first received section trace octet is J0 receive 15. The last received section trace octet is J0 receive 0. The J0 receive octets allow a WIS receiver to verify its continued connection to the intended transmitter. The received section trace is described in 50.3.2.4.

45.2.3 PCS registers

The assignment of registers in the PCS is shown in Table 45–65.

Table 45–65—PCS registers

Register address	Register name
3.0	PCS control 1
3.1	PCS status 1
3.2, 3.3	PCS device identifier
3.4	PCS speed ability
3.5, 3.6	PCS devices in package
3.7	10G PCS control 2
3.8	10G PCS status 2
3.9 through 3.13	Reserved
3.14, 3.15	PCS package identifier
3.16 through 3.23	Reserved
3.24	10GBASE-X PCS status
3.25	10GBASE-X PCS test control
3.26 through 3.31	Reserved
3.32	10GBASE-R PCS status 1
3.33	10GBASE-R PCS status 2
3.34 through 3.37	10GBASE-R PCS test pattern seed A
3.38 through 3.41	10GBASE-R PCS test pattern seed B
3.42	10GBASE-R PCS test pattern control
3.43	10GBASE-R PCS test pattern error counter
3.44 through 3.59	Reserved
3.60	10P/2B capability
3.61	10P/2B PCS control register
3.62, 3.63	10P/2B PME available
3.64, 3.65	10P/2B PME aggregate
3.66	10P/2B PAF RX error counter
3.67	10P/2B PAF small fragment counter
3.68	10P/2B PAF large fragments counter
3.69	10P/2B PAF overflow counter
3.70	10P/2B PAF bad fragments counter
3.71	10P/2B PAF lost fragments counter
3.72	10P/2B PAF lost starts of fragments counter
3.73	10P/2B PAF lost ends of fragments counter
3.74 through 3.32 767	Reserved
3.32 768 through 3.65 535	Vendor specific

45.2.3.1 PCS control 1 register (Register 3.0)

The assignment of bits in the PCS control 1 register is shown in Table 45–66. The default value for each bit of the PCS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–66—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.15	Reset	1 = PCS reset 0 = Normal operation	R/W SC
3.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.12	Reserved	Value always 0, writes ignored	R/W
3.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
3.0.10:7	Reserved	Value always 0, writes ignored	R/W
3.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
3.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.3.1.1 Reset (3.0.15)

Resetting a PCS is accomplished by setting bit 3.0.15 to a one. This action shall set all PCS registers to their default states. As a consequence, this action may change the internal state of the PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PCS shall return a value of one in bit 3.0.15 when a reset is in progress and a value of zero otherwise. A PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 3.0.15. During a reset, a PCS shall respond to reads from register bits 3.0.15 and 3.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.3.1.2 Loopback (3.0.14)

The 10GBASE-R PCS shall be placed in a loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 10GBASE-R PCS shall accept data on the transmit path and return it on the receive path. The specific behavior of the 10GBASE-R PCS during loopback is specified in 49.2. For all other port types, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

The default value of bit 3.0.14 is zero.

NOTE—The signal path through the PCS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PCS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.3.1.3 Low power (3.0.11)

A PCS may be placed into a low-power mode by setting bit 3.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PCS. The behavior of the PCS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 3.0.11 is zero.

45.2.3.1.4 Speed selection (3.0.13, 3.0.6, 3.0.5:2)

Speed selection bits 3.0.13 and 3.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PCS may be selected using bits 5 through 2. The speed abilities of the PCS are advertised in the PCS speed ability register. A PCS may ignore writes to the PCS speed selection bits that select speeds it has not advertised in the PCS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PCS speed selection defaults to a supported ability.

The speed selection bits 3.0.5:2, when set to 0001, select the use of the 10PASS-TS and 2BASE-TL PCS.

45.2.3.2 PCS status 1 register (Register 3.1)

The assignment of bits in the PCS status 1 register is shown in Table 45–67. All the bits in the PCS status 1 register are read only; a write to the PCS status 1 register shall have no effect.

45.2.3.2.1 Fault (3.1.7)

When read as a one, bit 3.1.7 indicates that the PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.1.7 indicates that the PCS has not detected a fault condition. For 10 Gb/s operation, bit 3.1.7 is read as a one when either of the fault bits (3.8.11, 3.8.10) located in register 3.8 are read as a one. For 10BASE-TS or 2BASE-TL operation, this bit shall become a one when any 10P/2B PCS registers indicate a fault (see 45.2.3.21 through 45.2.3.28).

Table 45–67—PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.1.15:8	Reserved	Ignore when read	RO
3.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.1.6:3	Reserved	Ignore when read	RO
3.1.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.1.1	Low-power ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO
3.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

45.2.3.2.2 PCS receive link status (3.1.2)

When read as a one, bit 3.1.2 indicates that the PCS receive link is up. When read as a zero, bit 3.1.2 indicates that the PCS receive link is down. When a 10GBASE-R or 10GBASE-W mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.32.12. When a 10GBASE-X mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.24.12. The receive link status bit shall be implemented with latching low behavior.

45.2.3.2.3 Low-power ability (3.1.1)

When read as a one, bit 3.1.1 indicates that the PCS supports the low-power feature. When read as a zero, bit 3.1.1 indicates that the PCS does not support the low-power feature. If a PCS supports the low-power feature then it is controlled using the low-power bit 3.0.11.

45.2.3.3 PCS device identifier (Registers 3.2 and 3.3)

Registers 3.2 and 3.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PCS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS device identifier.

The format of the PCS device identifier is specified in 22.2.4.3.1.

45.2.3.4 PCS speed ability (Register 3.4)

The assignment of bits in the PCS speed ability register is shown in Table 45–68.

45.2.3.4.1 10G capable (3.4.0)

When read as a one, bit 3.4.0 indicates that the PCS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 3.4.0 indicates that the PCS is not able to operate at a data rate of 10 Gb/s.

Table 45–68—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
3.4.1	10PASS-TS/2BASE-TL capable	1 = PCS is capable of operating as the 10P/2B PCS 0 = PCS is not capable of operating as the 10P/2B PCS	RO
3.4.0	10G capable	1 = PCS is capable of operating at 10 Gb/s 0 = PCS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.3.4.2 10PASS-TS/2BASE-TL capable

When read as a one, this bit indicates that the PCS is able to operate as the 10PASS-TS/2BASE-TL PCS, as specified in Clause 61.

45.2.3.5 PCS devices in package (Registers 3.5 and 3.6)

The PCS devices in package registers are defined in Table 45–2.

45.2.3.6 10G PCS control 2 register (Register 3.7)

The assignment of bits in the 10G PCS control 2 register is shown in Table 45–69. The default value for each bit of the 10G PCS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–69—10G PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:2	Reserved	Value always 0, writes ignored	R/W
3.7.1:0	PCS type selection	1 0 1 1 = Reserved 1 0 = Select 10GBASE-W PCS type 0 1 = Select 10GBASE-X PCS type 0 0 = Select 10GBASE-R PCS type	R/W

[a]R/W = Read/Write

45.2.3.6.1 PCS type selection (3.7.1:0)

The PCS type shall be selected using bits 1 through 0. The PCS type abilities of the 10G PCS are advertised in bits 3.8.2:0. A 10G PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the 10G PCS status 2 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

45.2.3.7 10G PCS status 2 register (Register 3.8)

The assignment of bits in the 10G PCS status 2 register is shown in Table 45–70. All the bits in the 10G PCS status 2 register are read only; a write to the 10G PCS status 2 register shall have no effect.

Table 45–70—10G PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
3.8.13:12	Reserved	Ignore when read	RO
3.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
3.8.10	Receive fault	1 = Fault condition on the receive path 0 = No fault condition on the receive path	RO/LH
3.8.9:3	Reserved	Ignore when read	RO
3.8.2	10GBASE-W capable	1 = PCS is able to support 10GBASE-W PCS type 0 = PCS is not able to support 10GBASE-W PCS type	RO
3.8.1	10GBASE-X capable	1 = PCS is able to support 10GBASE-X PCS type 0 = PCS is not able to support 10GBASE-X PCS type	RO
3.8.0	10GBASE-R capable	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types	RO

[a]RO = Read Only, LH = Latching High

45.2.3.7.1 Device present (3.8.15:14)

When read as <10>, bits 3.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 3.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

45.2.3.7.2 Transmit fault (3.8.11)

When read as a one, bit 3.8.11 indicates that the PCS has detected a fault condition on the transmit path. When read as a zero, bit 3.8.11 indicates that the PCS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.11 is zero.

45.2.3.7.3 Receive fault (3.8.10)

When read as a one, bit 3.8.10 indicates that the PCS has detected a fault condition on the receive path. When read as a zero, bit 3.8.10 indicates that the PCS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.10 is zero.

45.2.3.7.4 10GBASE-W capable (3.8.2)

When read as a one, bit 3.8.2 indicates that the 64B/66B PCS is able to support operation in a 10GBASE-W PHY (that is, supports operation with a WIS). When read as a zero, bit 3.8.2 indicates that the 64B/66B PCS is not able to support operation with a WIS in a 10GBASE-W PHY.

NOTE—This bit does not indicate that the PCS is performing the functionality contained in the WIS. This bit indicates whether the 64B/66B PCS would be able to support a WIS if it were to be attached.

45.2.3.7.5 10GBASE-X capable (3.8.1)

When read as a one, bit 3.8.1 indicates that the PCS is able to support the 10GBASE-X PCS type. When read as a zero, bit 3.8.1 indicates that the PCS is not able to support the 10GBASE-X PCS type.

45.2.3.7.6 10GBASE-R capable (3.8.0)

When read as a one, bit 3.8.0 indicates that the PCS is able to support operation in a 10GBASE-R PHY. When read as a zero, bit 3.8.0 indicates that the PCS is not able to support operation in a 10GBASE-R PHY.

45.2.3.8 PCS package identifier (Registers 3.14 and 3.15)

Registers 3.14 and 3.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PCS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

45.2.3.9 10GBASE-X PCS status register (Register 3.24)

The assignment of bits in the 10GBASE-X PCS status register is shown in Table 45–71. All the bits in the 10GBASE-X PCS status register are read only; a write to the 10GBASE-X PCS status register shall have no effect. A PCS device that does not implement 10GBASE-X shall return a zero for all bits in the 10GBASE-X PCS status register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

45.2.3.9.1 10GBASE-X receive lane alignment status (3.24.12)

When read as a one, bit 3.24.12 indicates that the 10GBASE-X PCS has synchronized and aligned all four receive lanes. When read as a zero, bit 3.24.12 indicates that the 10GBASE-X PCS has not synchronized and aligned all four receive lanes.

45.2.3.9.2 Pattern testing ability (3.24.11)

When read as a one, bit 3.24.11 indicates that the 10GBASE-X PCS is able to generate test patterns. When read as a zero, bit 3.24.11 indicates that the 10GBASE-X PCS is not able to generate test patterns. If the 10GBASE-X PCS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 3.25.

Table 45–71—10GBASE-X PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.24.15:13	Reserved	Ignore when read	RO
3.24.12	10GBASE-X lane alignment status	1 = 10GBASE-X PCS receive lanes aligned 0 = 10GBASE-X PCS receive lanes not aligned	RO
3.24.11	Pattern testing ability	1 = 10GBASE-X PCS is able to generate test patterns 0 = 10GBASE-X PCS is not able to generate test patterns	RO
3.24.10:4	Reserved	Ignore when read	RO
3.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
3.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
3.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
3.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.3.9.3 Lane 3 sync (3.24.3)

When read as a one, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is synchronized. When read as a zero, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is not synchronized.

45.2.3.9.4 Lane 2 sync (3.24.2)

When read as a one, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is synchronized. When read as a zero, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is not synchronized.

45.2.3.9.5 Lane 1 sync (3.24.1)

When read as a one, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is synchronized. When read as a zero, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is not synchronized.

45.2.3.9.6 Lane 0 sync (3.24.0)

When read as a one, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is synchronized. When read as a zero, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is not synchronized.

45.2.3.10 10GBASE-X PCS test control register (Register 3.25)

The assignment of bits in the 10GBASE-X PCS test control register is shown in Table 45–72. The default value for each bit of the 10GBASE-X PCS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–72—10GBASE-X PCS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.25.15:3	Reserved	Value always 0, writes ignored	R/W
3.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W
3.25.1:0	Test pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

45.2.3.10.1 Transmit test-pattern enable (3.25.2)

When bit 3.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 3.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10GBASE-X PCS to generate test patterns is advertised by the pattern testing ability bit in register 3.24. A 10GBASE-X PCS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 3.25.2 is zero.

45.2.3.10.2 Test pattern select (3.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 3.25.2 is selected using bits 3.25.1:0. When bits 3.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.3.11 10GBASE-R PCS status 1 register (Register 3.32)

The assignment of bits in the 10GBASE-R PCS status 1 register is shown in Table 45–73. All the bits in the 10GBASE-R PCS status 1 register are read only; a write to the 10GBASE-R PCS status 1 register shall have no effect. A PCS device that does not implement 10GBASE-R shall return a zero for all bits in the 10GBASE-R PCS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.32 are undefined when the 10GBASE-R PCS is operating in seed test-pattern mode or PRBS31 test-pattern mode.

45.2.3.11.1 10GBASE-R receive link status (3.32.12)

When read as a one, bit 3.32.12 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.32.12 indicates that the PCS is not fully operational. This bit is a reflection of the state of the PCS_status variable defined in 49.2.14.1.

45.2.3.11.2 PRBS31 pattern testing ability (3.32.2)

When read as a one, bit 3.32.2 indicates that the PCS is able to support PRBS31 pattern testing. When read as a zero, bit 3.32.2 indicates that the PCS is not able to support PRBS31 pattern testing. If the PCS is able to support PRBS31 pattern testing then the pattern generation and checking is controlled using bits 3.42.5:4.

Table 45–73—10GBASE-R PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.32.15:13	Reserved	Ignore when read	RO
3.32.12	10GBASE-R receive link status	1 = 10GBASE-R PCS receive link up 0 = 10GBASE-R PCS receive link down	RO
3.32.11:3	Reserved	Ignore when read	RO
3.32.2	PRBS31 pattern testing ability	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing	RO
3.32.1	10GBASE-R PCS high BER	1 = 10GBASE-R PCS reporting a high BER 0 = 10GBASE-R PCS not reporting a high BER	RO
3.32.0	10GBASE-R PCS block lock	1 = 10GBASE-R PCS locked to received blocks 0 = 10GBASE-R PCS not locked to received blocks	RO

[a]RO = Read Only

45.2.3.11.3 10GBASE-R PCS high BER (3.32.1)

When read as a one, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_ber variable in the 64B/66B state machine and is defined in 49.2.13.2.2.

45.2.3.11.4 10GBASE-R PCS block lock (3.32.0)

When read as a one, bit 3.32.0 indicates that the 64B/66B receiver has block lock. When read as a zero, bit 3.32.0 indicates that the 64B/66B receiver has not got block lock. This bit is a direct reflection of the state of the block_lock variable in the 64B/66B state machine and is defined in 49.2.13.2.2.

45.2.3.12 10GBASE-R PCS status 2 register (Register 3.33)

The assignment of bits in the 10GBASE-R PCS status 2 register is shown in Table 45–74. All the bits in the 10GBASE-R PCS status 2 register are read only; a write to the 10GBASE-R PCS status 2 register shall have no effect. A PCS device which does not implement 10GBASE-R shall return a zero for all bits in the 10GBASE-R PCS status 2 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.33 are undefined when the 10GBASE-R PCS is operating in seed test-pattern mode or PRBS31 test-pattern mode.

Table 45–74—10GBASE-R PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.33.15	Latched block lock	1 = 10GBASE-R PCS has block lock 0 = 10GBASE-R PCS does not have block lock	RO/LL
3.33.14	Latched high BER	1 = 10GBASE-R PCS has reported a high BER 0 = 10GBASE-R PCS has not reported a high BER	RO/LH
3.33.13:8	BER	BER counter	RO/NR
3.33.7:0	Errored blocks	Errored blocks counter	RO/NR

[a]RO = Read Only, LL = Latching Low, LH = Latching High, NR = Non Roll-over

45.2.3.12.1 Latched block lock (3.33.15)

When read as a one, bit 3.33.15 indicates that the 10GBASE-R PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 10GBASE-R PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 10GBASE-R PCS block lock status bit (3.32.0).

45.2.3.12.2 Latched high BER (3.33.14)

When read as a one, bit 3.33.14 indicates that the 10GBASE-R PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 10GBASE-R PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 10GBASE-R PCS high BER status bit (3.32.1).

45.2.3.12.3 BER(3.33.13:8)

The BER counter is a six bit count as defined by the ber_count variable in 49.2.14.2. These bits shall be reset to all zeros when the BER count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.12.4 Errored blocks (3.33.7:0)

The errored blocks counter is an eight bit count defined by the errored_block_count counter specified in 49.2.14.2. These bits shall be reset to all zeros when the errored blocks count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.13 10GBASE-R PCS test pattern seed A (Registers 3.34 through 3.37)

The assignment of bits in the 10GBASE-R PCS test pattern seed A registers is shown in Table 45–75. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are

assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

Table 45–75—10GBASE-R PCS test pattern seed A 0-3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.37.15:10	Reserved	Value always 0, writes ignored	R/W
3.37.9:0	Test pattern seed A 3	Test pattern seed A bits 48-57	R/W
3.36.15:0	Test pattern seed A 2	Test pattern seed A bits 32-47	R/W
3.35.15:0	Test pattern seed A 1	Test pattern seed A bits 16-31	R/W
3.34.15:0	Test pattern seed A 0	Test pattern seed A bits 0-15	R/W

[a]R/W = Read/Write

The A seed for the pseudo random test pattern is held in registers 3.34 through 3.37. The test-pattern methodology is described in 49.2.8.

45.2.3.14 10GBASE-R PCS test pattern seed B (Registers 3.38 through 3.41)

The assignment of bits in the 10GBASE-R PCS test pattern seed B registers is shown in Table 45–76. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

Table 45–76—10GBASE-R PCS test pattern seed B 0-3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.41.15:10	Reserved	Value always 0, writes ignored	R/W
3.41.9:0	Test pattern seed B 3	Test pattern seed B bits 48-57	R/W
3.40.15:0	Test pattern seed B 2	Test pattern seed B bits 32-47	R/W
3.39.15:0	Test pattern seed B 1	Test pattern seed B bits 16-31	R/W
3.38.15:0	Test pattern seed B 0	Test pattern seed B bits 0-15	R/W

[a]R/W = Read/Write

The B seed for the pseudo random test pattern is held in registers 3.38 through 3.41. The test-pattern methodology is described in 49.2.8.

45.2.3.15 10GBASE-R PCS test-pattern control register (Register 3.42)

The assignment of bits in the 10GBASE-R PCS test-pattern control register is shown in Table 45–77. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. The test-pattern methodology is described in 49.2.8.

Table 45–77—10GBASE-R PCS test-pattern control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.42.15:6	Reserved	Value always 0, writes ignored	R/W
3.42.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
3.42.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
3.42.3	Transmit test-pattern enable	1 = Enable transmit test pattern 0 = Disable transmit test pattern	R/W
3.42.2	Receive test-pattern enable	1 = Enable receive test-pattern testing 0 = Disable receive test-pattern testing	R/W
3.42.1	Test-pattern select	1 = Square wave test pattern 0 = Pseudo random test pattern	R/W
3.42.0	Data pattern select	1 = Zeros data pattern 0 = LF data pattern	R/W

[a]R/W = Read/Write

45.2.3.15.1 PRBS31 receive test-pattern enable (3.42.5)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory receive test-pattern enable bit (3.42.2) is not one, setting bit 3.42.5 to a one shall set the receive path of the PCS into the PRBS31 test-pattern mode. The number of errors received during a PRBS31 pattern test are recorded in register 3.43. Setting bit 3.42.5 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49

45.2.3.15.2 PRBS31 transmit test-pattern enable (3.42.4)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory transmit test-pattern enable bit (3.42.3) is not one, then setting bit 3.42.4 to a one shall set the transmit path of the PCS into the PRBS31 test-pattern mode. Setting bit 3.42.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49

45.2.3.15.3 Transmit test-pattern enable (3.42.3)

When bit 3.42.3 is set to a one, pattern testing is enabled on the transmit path. When bit 3.42.3 is set to a zero, pattern testing is disabled on the transmit path.

The default value for bit 3.42.3 is zero.

45.2.3.15.4 Receive test-pattern enable (3.42.2)

When bit 3.42.2 is set to a one, pattern testing is enabled on the receive path. When bit 3.42.2 is set to a zero, pattern testing is disabled on the receive path.

The default value for bit 3.42.2 is zero.

45.2.3.15.5 Test-pattern select (3.42.1)

When bit 3.42.1 is set to a one, the square wave test pattern is used for pattern testing. When bit 3.42.1 is set to a zero, the pseudo random test pattern is used for pattern testing.

The default value for bit 3.42.1 is zero.

45.2.3.15.6 Data pattern select (3.42.0)

When bit 3.42.0 is set to a one, the zeros data pattern is used for pattern testing. When bit 3.42.0 is set to a zero, the LF data pattern is used for pattern testing.

The default value for bit 3.42.0 is zero.

45.2.3.16 10GBASE-R PCS test-pattern error counter register (Register 3.43)

The assignment of bits in the 10GBASE-R PCS test-pattern error counter register is shown in Table 45–78. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode, or may function as defined for 10GBASE-R.

Table 45–78—10GBASE-R PCS test-pattern error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.43.15:0	Test-pattern error counter	Error counter	RO

[a]RO = Read Only

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.12. This counter will count either block errors or bit errors dependent on the test mode (see 49.2.12).

45.2.3.17 10P/2B capability register (3.60)

The 10P/2B capability register reports which functions are supported by the PCS. This register is present at the PCS layer for each PHY. The bit definitions of the 10P/2B capability register are shown in Table 45–79.

45.2.3.17.1 PAF available (3.60.12)

This bit indicates that the PHY supports the PME aggregation function. The PHY sets this bit to a one when the capability is supported and zero otherwise. This bit reflects the signal PAF_available in 61.2.3.

Table 45–79—10P/2B capability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.60.15:13	Reserved	Value always 0, writes ignored	RO
3.60.12	PAF available	1 = PAF supported 0 = PAF not supported	RO
3.60.11	Remote PAF supported	1 = link partner supports PAF 0 = link partner does not support PAF	RO
3.60.10:0	Reserved	Value always 0, writes ignored	RO

[a]**RO = Read Only**

45.2.3.17.2 Remote PAF supported (3.60.11)

This bit indicates that the remote, link-partner PHY supports the PME aggregation function. The PHY sets this bit to a one when the capability is supported and zero otherwise. This bit does not accurately report the capability of the remote PCS until a remote discovery operation has been completed by the -O PHY. In this case, this bit is set if the “Ethernet bonding” NPar(2) bit is set in the capabilities exchange message received from the other device. See 61.4.7, which discusses use of G.994.1 to access remote registers.

45.2.3.18 10P/2B PCS control register (Register 3.61)

The assignment of bits in the 10P/2B PCS control register is shown in Table 45–80.

Table 45–80—10B/2B PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.61.15	MII receive during transmit	1 = MII can TX/RX simultaneously 0 = MII cannot TX/RX simultaneously (default)	R/W
3.61.14	TX_EN and CRS infer a collision	1 = MII uses TX_EN and CRS to infer a collision 0 = MII uses COL to indicate a collision (default)	R/W
3.61.13:1	Reserved	Value always 0, writes ignored	R/W
3.61.0	PAF enable	1 = use PAF 0 = do not use PAF	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.3.18.1 MII receive during transmit (3.61.15)

This register bit is used to tell the PHY-MAC rate matching function if the MAC is capable of receiving frames from the PHY while the MAC is transmitting (i.e., sending frames to the PHY). The variable tx_rx_simultaneously for the PHY-MAC Rate-Matching function takes on the value of this bit as defined in 61.2.3.

45.2.3.18.2 TX_EN and CRS infer a collision (3.61.14)

This bit is set by the STA to tell the MAC-PHY rate matching function that the MAC-PHY interface does not have a separate collision signal but instead infers a collision when TX_EN and CRS are asserted

simultaneously. The variable crs_and_tx_en_infer_col in the PHY-MAC Rate-Matching function takes on the value of this bit as in 61.2.3. This bit will default to a supported mode, and writes to unsupported modes will be ignored.

45.2.3.18.3 PAF enable (3.61.0)

Setting this bit to a one shall activate the PME aggregation function of the PCS when the link is established. Writes to this bit while link is up or initializing (see 45.2.1.12) or if the PAF is not supported shall be ignored. When link is established, handshake indicates the use of PAF to the -R PHY. This bit reflects the signal PAF_enable in 61.2.3.4.

45.2.3.19 10P/2B PME available (Registers 3.62 and 3.63)

The 10P/2B PME available registers are used to indicate which PMEs in the aggregation group are available to be attached to the queried PCS. A PME is marked as unavailable if the PME does not support PME aggregation or if the PME is currently marked to be aggregated with another PMD. For a device that does not support aggregation of multiple PMEs, a single bit of this register shall be set to one and all other bits cleared to zero.

These registers may be writeable for -R ports. For PMEs that may be accessed through more than one MII, the availability is limited such that no PME may be mapped to more than one MII prior to enabling the links. In this case, the reset state of the 10P/2B PME available registers shall reflect the capabilities of the device, the management entity should reset appropriate bits to meet the restriction described.

If the -R device is not capable of aggregating PMEs to multiple MIIs then these registers may be read only.

The 10P/2B PME available register shall be available per PCS. For example, a package implementing four PMEs and one MII would have only one set of 10P/2B PME available registers, addressed by a read or write to 3.62 and 3.63 on any of those PHYs.

For more information, see 61.2.2.8.3.

The assignment of bits in the 10P/2B PME available registers is shown in Table 45–81.

45.2.3.20 10P/2B PME aggregate registers (Registers 3.64 and 3.65)

Table 45–81—10P/2B PME available register bit definitions

Bit(s)	Name	Description	R/W[a]
3.62.15:0	PME [p = 31:16] available	For each bit in the sequence: 1 = PME[p] is available for aggregating 0 = PME[p] is unavailable	O: RO R: R/W
3.63.15:0	PME [p = 15:0] available	For each bit in the sequence: 1 = PME[p] is available for aggregating 0 = PME[p] is unavailable	O: RO R: R/W

[a]RO = Read Only, R/W = Read/Write

The 10P/2B PME aggregate registers are used to select PMEs for aggregation. Attempts to activate aggregation with an unavailable PME (see 45.2.3.19) are ignored. The PCS shall use PME aggregation if one or more bits are set to a one and if PME aggregation is supported.

The 10P/2B PME aggregate register shall be available per PCS. For example, a package implementing four PMEs and one MII would have only one set of 10P/2B PME aggregate registers, accessed by a read or write to 3.64, 3.65 on any of those PHYs.

Upon MMD reset, these registers shall be reset to all zeros.

For more information, see 61.2.2.8.3.

The assignment of bits for the 10P/2B PME aggregate registers are shown in Table 45–82.

Table 45–82—10P/2B PME aggregate register bit definitions

Bit(s)	Name	Description	R/W[a]
3.64.15:0	Aggregate with PME [p = 31:16]	For each bit in the sequence: 1 = activate aggregation with PME[p] 0 = deactivate aggregation with PME[p]	R/W
3.65.15:0	Aggregate with PME [p = 15:0]	For each bit in the sequence: 1 = activate aggregation with PME[p] 0 = deactivate aggregation with PME[p]	R/W

[a]R/W = Read/Write

45.2.3.21 10P/2B PAF RX error register (Register 3.66)

The 10P/2B PAF RX error register is a 16 bit counter that contains the number of fragments that have been received across the gamma interface with RxErr asserted. The corresponding signal, TC_PAF_RxErrorReceived, is defined in 61.2.3. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be reset to all zeros when the 10P/2B PAF RX error register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF RX error register is shown in Table 45–83.

Table 45–83—10P/2B PAF RX error register bit definitions

Bit(s)	Name	Description	R/W[a]
3.66.15:0	PAF RX errors[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.22 10P/2B PAF small fragments register (Register 3.67)

The 10P/2B PAF small fragments register is a 16 bit counter that contains the number of small fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_FragmentTooSmall, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits

shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF small fragment register is shown in Table 45–84.

Table 45–84—10P/2B PAF small fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.67.15:0	PAF small fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.23 10P/2B PAF large fragments register (Register 3.68)

The 10P/2B PAF large fragments register is a 16 bit counter that contains the number of large fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_FragmentTooLarge, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF large fragments register is shown in Table 45–85.

Table 45–85—10P/2B PAF large fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.68.15:0	PAF large fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.24 10P/2B PAF overflow register (Register 3.69)

The 10P/2B PAF overflow register is a 16 bit counter that contains the number of fragments that have been received across the gamma interface which would have caused the receive buffer to overflow. The corresponding signal, TC_PAF_Overflow, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF overflow register is shown in Table 45–86.

Table 45–86—10P/2B PAF overflow register bit definitions

Bit(s)	Name	Description	R/W[a]
3.69.15:0	PAF overflow fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.25 10P/2B PAF bad fragments register (Register 3.70)

The 10P/2B PAF bad fragments register is a 16 bit counter that contains the number of bad fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_BadFragmentReceived, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones

in the case of overflow. The assignment of bits in the 10P/2B PAF bad fragments register is shown in Table 45–87.

Table 45–87—P10P/2B AF bad fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.70.15:0	PAF bad fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.26 10P/2B PAF lost fragments register (Register 3.71)

The 10P/2B PAF lost fragments register is a 16 bit counter that contains the number of gaps in the sequence of fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_LostFragment, is defined in 61.2.3.

These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost fragments register is shown in Table 45–88.

Table 45–88—10P/2B PAF lost fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.71.15:0	PAF lost fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.27 10P/2B PAF lost starts of fragments register (Register 3.72)

The 10P/2B PAF lost starts of fragments register is a 16-bit counter that contains the number of missing start of fragment indicators expected by the frame assembly function. The corresponding signal, TC_PAF_LostStart, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost starts of fragments register is shown in Table 45–89.

Table 45–89—10P/2B PAF lost starts of fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.72.15:0	PAF lost starts of fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.28 10P/2B PAF lost ends of fragments register (Register 3.73)

The 10P/2B PAF lost ends of fragments register is a 16 bit counter that contains the number of missing end of fragment indicators expected by the frame assembly function. The corresponding signal, TC_PAF_LostEnd, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the

management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost ends of fragments register is shown in Table 45–90.

Table 45–90—10P/2B PAF lost ends of fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.73.15:0	PAF lost ends of fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.4 PHY XS registers

The assignment of registers in the PHY XS is shown in Table 45–91.

Table 45–91—PHY XS registers

Register address	Register name
4.0	PHY XS control 1
4.1	PHY XS status 1
4.2, 4.3	PHY XS device identifier
4.4	PHY XS speed ability
4.5, 4.6	PHY XS devices in package
4.7	Reserved
4.8	PHY XS status 2
4.9 through 4.13	Reserved
4.14, 4.15	PHY XS package identifier
4.16 through 4.23	Reserved
4.24	10G PHY XGXS lane status
4.25	10G PHY XGXS test control
4.26 through 4.32 767	Reserved
4.32 768 through 4.65 535	Vendor specific

45.2.4.1 PHY XS control 1 register (Register 4.0)

The assignment of bits in the PHY XS control 1 register is shown in Table 45–92. The default value for each bit of the PHY XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–92—PHY XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.0.15	Reset	1 = PHY XS reset 0 = Normal operation	R/W SC
4.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
4.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.12	Reserved	Value always 0, writes ignored	R/W
4.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
4.0.10:7	Reserved	Value always 0, writes ignored	R/W
4.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
4.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.4.1.1 Reset (4.0.15)

Resetting a PHY XS is accomplished by setting bit 4.0.15 to a one. This action shall set all PHY XS registers to their default states. As a consequence, this action may change the internal state of the PHY XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PHY XS shall return a value of one in bit 4.0.15 when a reset is in progress and a value of zero otherwise. A PHY XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 4.0.15. During a reset, a PHY XS shall respond to reads from register bits 4.0.15 and 4.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.4.1.2 Loopback (4.0.14)

The PHY XS shall be placed in a loopback mode of operation when bit 4.0.14 is set to a one. When bit 4.0.14 is set to a one, the PHY XS shall accept data on the receive path and return it on the transmit path. The direction of the loopback path for the PHY XS is opposite to all other MMD loopbacks.

The loopback function is optional. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PHY XS that is unable to perform the loopback function shall ignore writes to this bit and return a value of zero when read. For 10 Gb/s operation,

the loopback functionality is detailed in 48.3.3 and the loopback ability bit is specified in the 10G PHY XGXS Lane status register.

The default value of bit 4.0.14 is zero.

NOTE—The signal path through the PHY XS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY XS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.4.1.3 Low power (4.0.11)

A PHY XS may be placed into a low-power mode by setting bit 4.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PHY XS. The behavior of the PHY XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 4.0.11 is zero.

45.2.4.1.4 Speed selection (4.0.13, 4.0.6, 4.0.5:2)

Speed selection bits 4.0.13 and 4.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PHY XS may be selected using bits 5 through 2. The speed abilities of the PHY XS are advertised in the PHY XS speed ability register. A PHY XS may ignore writes to the PHY XS speed selection bits that select speeds it has not advertised in the PHY XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PHY XS speed selection defaults to a supported ability.

45.2.4.2 PHY XS status 1 register (Register 4.1)

The assignment of bits in the PHY XS status 1 register is shown in Table 45–93. All the bits in the PHY XS status 1 register are read only; a write to the PHY XS status 1 register shall have no effect.

45.2.4.2.1 Fault (4.1.7)

When read as a one, bit 4.1.7 indicates that the PHY XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 4.1.7 indicates that the PHY XS has not detected a fault condition. Bit 4.1.7 is set to a one when either of the fault bits (4.8.11, 4.8.10) located in register 4.8 are set to a one.

45.2.4.2.2 PHY XS transmit link status (4.1.2)

When read as a one, bit 4.1.2 indicates that the PHY XS transmit link is aligned. When read as a zero, bit 4.1.2 indicates that the PHY XS transmit link is not aligned. The transmit link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, bit 4.1.2 is a latching low version of bit 4.24.12.

Table 45–93—PHY XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.1.15:8	Reserved	Ignore when read	RO
4.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
4.1.6:3	Reserved	Ignore when read	RO
4.1.2	PHY XS transmit link status	1 = The PHY XS transmit link is up 0 = The PHY XS transmit link is down	RO/LL
4.1.1	Low-power ability	1 = PHY XS supports low-power mode 0 = PHY XS does not support low-power mode	RO
4.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

45.2.4.2.3 Low-power ability (4.1.1)

When read as a one, bit 4.1.1 indicates that the PHY XS supports the low-power feature. When read as a zero, bit 4.1.1 indicates that the PHY XS does not support the low-power feature. If a PHY XS supports the low-power feature then it is controlled using the low-power bit in the PHY XS control register.

45.2.4.3 PHY XS device identifier (Registers 4.2 and 4.3)

Registers 4.2 and 4.3 provide a 32-bit value, which may constitute a unique identifier for a PHY XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS device identifier.

The format of the PHY XS device identifier is specified in 22.2.4.3.1.

45.2.4.4 PHY XS speed ability (Register 4.4)

The assignment of bits in the PHY XS speed ability register is shown in Table 45–94.

Table 45–94—PHY XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
4.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
4.4.0	10G capable	1 = PHY XS is capable of operating at 10 Gb/s 0 = PHY XS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.4.4.1 10G capable (4.4.0)

When read as a one, bit 4.4.0 indicates that the PHY XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 4.4.0 indicates that the PHY-XS is not able to operate at a data rate of 10 Gb/s.

45.2.4.5 PHY XS devices in package (Registers 4.5 and 4.6)

The PHY XS devices in package registers are defined in Table 45–2.

45.2.4.6 PHY XS status 2 register (Register 4.8)

The assignment of bits in the PHY XS status 2 register is shown in Table 45–95. All the bits in the PHY XS status 2 register are read only; a write to the PHY XS status 2 register shall have no effect.

Table 45–95—PHY XS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
4.8.13:12	Reserved	Ignore when read	RO
4.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
4.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
4.8.9:0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High

45.2.4.6.1 Device present (4.8.15:14)

When read as <10>, bits 4.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 4.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.4.6.2 Transmit fault (4.8.11)

When read as a one, bit 4.8.11 indicates that the PHY XS has detected a fault condition on the transmit path. When read as a zero, bit 4.8.11 indicates that the PHY XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value for bit 4.8.11 is zero.

45.2.4.6.3 Receive fault (4.8.10)

When read as a one, bit 4.8.10 indicates that the PHY XS has detected a fault condition on the receive path. When read as a zero, bit 4.8.10 indicates that the PHY XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 4.8.10 is zero.

45.2.4.7 PHY XS package identifier (Registers 4.14 and 4.15)

Registers 4.14 and 4.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PHY XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the PHY XS package identifier is specified in 22.2.4.3.1.

45.2.4.8 10G PHY XGXS lane status register (Register 4.24)

The assignment of bits in the 10G PHY XGXS lane status register is shown in Table 45–96. All the bits in the 10G PHY XGXS lane status register are read only; a write to the 10G PHY XGXS lane status register shall have no effect.

45.2.4.8.1 PHY XGXS transmit lane alignment status (4.24.12)

When read as a one, bit 4.24.12 indicates that the PHY XGXS has synchronized and aligned all four transmit lanes. When read as a zero, bit 4.24.12 indicates that the PHY XGXS has not synchronized and aligned all four transmit lanes.

45.2.4.8.2 Pattern testing ability (4.24.11)

When read as a one, bit 4.24.11 indicates that the 10G PHY XGXS is able to generate test patterns. When read as a zero, bit 4.24.11 indicates that the 10G PHY XGXS is not able to generate test patterns. If the 10G PHY XGXS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 4.25.

45.2.4.8.3 PHY XS loopback ability (4.24.10)

When read as a one, bit 4.24.10 indicates that the PHY XGXS is able to perform the loopback function. When read as a zero, bit 4.24.10 indicates that the PHY XGXS is not able to perform the loopback function. If a 10G PHY XGXS is able to perform the loopback function, then it is controlled using the PHY XGXS loopback bit 4.0.14.

45.2.4.8.4 Lane 3 sync (4.24.3)

When read as a one, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is synchronized. When read as a zero, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is not synchronized.

Table 45–96—10G PHY XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
4.24.15:13	Reserved	Ignore when read	RO
4.24.12	PHY XGXS lane alignment status	1 = PHY XGXS transmit lanes aligned 0 = PHY XGXS transmit lanes not aligned	RO
4.24.11	Pattern testing ability	1 = PHY XGXS is able to generate test patterns 0 = PHY XGXS is not able to generate test patterns	RO
4.24.10	PHY XGXS loopback ability	1 = PHY XGXS has the ability to perform a loopback function 0 = PHY XGXS does not have the ability to perform a loopback function	RO
4.24.9:4	Reserved	Ignore when read	RO
4.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
4.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
4.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
4.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.4.8.5 Lane 2 sync (4.24.2)

When read as a one, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is synchronized. When read as a zero, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is not synchronized.

45.2.4.8.6 Lane 1 sync (4.24.1)

When read as a one, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is synchronized. When read as a zero, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is not synchronized.

45.2.4.8.7 Lane 0 sync (4.24.0)

When read as a one, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is synchronized. When read as a zero, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is not synchronized.

45.2.4.9 10G PHY XGXS test control register (Register 4.25)

The assignment of bits in the 10G PHY XGXS test control register is shown in Table 45–97. The default value for each bit of the 10G PHY XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–97—10G PHY XGXS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
4.25.15:3	Reserved	Value always 0, writes ignored	R/W
4.25.2	Receive test-pattern enable	1 = Receive test pattern enabled 0 = Receive test pattern not enabled	R/W
4.25.1:0	Test-pattern select	1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

45.2.4.9.1 10G PHY XGXS test-pattern enable (4.25.2)

When bit 4.25.2 is set to a one, pattern testing is enabled on the receive path. When bit 4.25.2 is set to a zero, pattern testing is disabled on the receive path. Pattern testing is optional, and the ability of the 10G PHY XGXS to generate test patterns is advertised by the pattern testing ability bit in register 4.24. A 10G PHY XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 4.25.2 is zero.

45.2.4.9.2 10G PHY XGXS test-pattern select (4.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 4.25.2 is selected using bits 4.25.1:0. When bits 4.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.5 DTE XS registers

The assignment of registers in the DTE XS is shown in Table 45–98.

45.2.5.1 DTE XS control 1 register (Register 5.0)

The assignment of bits in the DTE XS control 1 register is shown in Table 45–99. The default value for each bit of the DTE XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.5.1.1 Reset (5.0.15)

Resetting a DTE XS is accomplished by setting bit 5.0.15 to a one. This action shall set all DTE XS registers to their default states. As a consequence, this action may change the internal state of the DTE XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a DTE XS shall return a value of one in bit 5.0.15 when a reset is in progress and a value of zero otherwise. A DTE XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 5.0.15. During a reset, a DTE XS shall respond to reads to register bits 5.0.15 and 5.8.15:14. All other register bits should be ignored.

Table 45–98—DTE XS registers

Register address	Register name
5.0	DTE XS control 1
5.1	DTE XS status 1
5.2, 5.3	DTE XS device identifier
5.4	DTE XS speed ability
5.5, 5.6	DTE XS devices in package
5.7	Reserved
5.8	DTE XS status 2
5.9 through 5.13	Reserved
5.14, 5.15	DTE XS package identifier
5.16 through 5.23	Reserved
5.24	10G DTE XGXS lane status
5.25	10G DTE XGXS test control
5.26 through 5.32 767	Reserved
5.32 768 through 5.65 535	Vendor specific

NOTE—This operation may interrupt data communication.

45.2.5.1.2 Loopback (5.0.14)

The DTE XS shall be placed in a loopback mode of operation when bit 5.0.14 is set to a one. When bit 5.0.14 is set to a one, the DTE XS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the specific behavior of a DTE XS during loopback is specified in 48.3.3.

The default value of bit 5.0.14 is zero.

NOTE—The signal path through the DTE XS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the DTE XS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.5.1.3 Low power (5.0.11)

A DTE XS may be placed into a low-power mode by setting bit 5.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the DTE XS. The behavior of the DTE XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 5.0.11 is zero.

Table 45–99—DTE XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.0.15	Reset	1 = DTE XS reset 0 = Normal operation	R/W SC
5.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
5.0.13	Speed selection	1 = Operation at 10 Gbp/s and above 0 = Unspecified	R/W
5.0.12	Reserved	Value always 0, writes ignored	R/W
5.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
5.0.10:7	Reserved	Value always 0, writes ignored	R/W
5.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
5.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
5.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.5.1.4 Speed selection (5.0.13, 5.0.6, 5.0.5:2)

Speed selection bits 5.0.13 and 5.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the DTE XS may be selected using bits 5 through 2. The speed abilities of the DTE XS are advertised in the DTE XS speed ability register. A DTE XS may ignore writes to the DTE XS speed selection bits that select speeds it has not advertised in the DTE XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The DTE XS speed selection defaults to a supported ability.

45.2.5.2 DTE XS status 1 register (Register 5.1)

The assignment of bits in the DTE XS status 1 register is shown in Table 45–100. All the bits in the DTE XS status 1 register are read only; a write to the DTE XS status 1 register shall have no effect.

Table 45–100—DTE XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.1.15:8	Reserved	Ignore when read	RO
5.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
5.1.6:3	Reserved	Ignore when read	RO
5.1.2	DTE XS receive link status	1 = The DTE XS receive link is up 0 = The DTE XS receive link is down	RO/LL
5.1.1	Low-power ability	1 = DTE XS supports low-power mode 0 = DTE XS does not support low-power mode	RO
5.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

45.2.5.2.1 Fault (5.1.7)

When read as a one, bit 5.1.7 indicates that the DTE XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 5.1.7 indicates that the DTE XS has not detected a fault condition. Bit 5.1.7 is set to a one when either of the fault bits (5.8.11, 5.8.10) located in register 5.8 are set to a one.

45.2.5.2.2 DTE XS receive link status (5.1.2)

When read as a one, bit 5.1.2 indicates that the DTE XS receive link is aligned. When read as a zero, bit 5.1.2 indicates that the DTE XS receive link is not aligned. The receive link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, this bit is a latching low version of bit 5.24.12.

45.2.5.2.3 Low-power ability (5.1.1)

When read as a one, bit 5.1.1 indicates that the DTE XS supports the low-power feature. When read as a zero, bit 5.1.1 indicates that the DTE XS does not support the low-power feature. If a DTE XS supports the low-power feature then it is controlled using the low-power bit in the DTE XS control register.

45.2.5.3 DTE XS device identifier (Registers 5.2 and 5.3)

Registers 5.2 and 5.3 provide a 32-bit value, which may constitute a unique identifier for a DTE XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS device identifier.

The format of the DTE XS device identifier is specified in 22.2.4.3.1

45.2.5.4 DTE XS speed ability (Register 5.4)

The assignment of bits in the DTE XS speed ability register is shown in Table 45–101.

Table 45–101— DTE XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
5.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
5.4.0	10G capable	1 = DTE XS is capable of operating at 10 Gb/s 0 = DTE XS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.5.4.1 10G capable (5.4.0)

When read as a one, bit 5.4.0 indicates that the DTE XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 5.4.0 indicates that the DTE XS is not able to operate at a data rate of 10 Gb/s.

45.2.5.5 DTE XS devices in package (Registers 5.5 and 5.6)

The DTE XS devices in package registers are defined in Table 45–2.

45.2.5.6 DTE XS status 2 register (Register 5.8)

The assignment of bits in the DTE XS status 2 register is shown in Table 45–102. All the bits in the DTE XS status 2 register are read only; a write to the DTE XS status 2 register shall have no effect.

Table 45–102—DTE XS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
5.8.13:12	Reserved	Ignore when read	RO
5.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
5.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
5.8.9:0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High

45.2.5.6.1 Device present (5.8.15:14)

When read as <10>, bits 5.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 5.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.5.6.2 Transmit fault (5.8.11)

When read as a one, bit 5.8.11 indicates that the DTE XS has detected a fault condition on the transmit path. When read as a zero, bit 5.8.11 indicates that the DTE XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 5.8.11 is zero.

45.2.5.6.3 Receive fault (5.8.10)

When read as a one, bit 5.8.10 indicates that the DTE XS has detected a fault condition on the receive path. When read as a zero, bit 5.8.10 indicates that the DTE XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 5.8.10 is zero.

45.2.5.7 DTE XS package identifier (Registers 5.14 and 5.15)

Registers 5.14 and 5.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the DTE XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the DTE XS package identifier is specified in 22.2.4.3.1.

45.2.5.8 10G DTE XGXS lane status register (Register 5.24)

The assignment of bits in the 10G DTE XGXS lane status register is shown in Table 45–103. All the bits in the 10G DTE XGXS lane status register are read only; a write to the 10G DTE XGXS lane status register shall have no effect.

45.2.5.8.1 DTE XGXS receive lane alignment status (5.24.12)

When read as a one, bit 5.24.12 indicates that the DTE XGXS has synchronized and aligned all four receive lanes. When read as a zero, bit 5.24.12 indicates that the DTE XGXS has not synchronized and aligned all four receive lanes.

45.2.5.8.2 Pattern testing ability (5.24.11)

When read as a one, bit 5.24.11 indicates that the 10G DTE XGXS is able to generate test patterns. When read as a zero, bit 5.24.11 indicates that the 10G DTE XGXS is not able to generate test patterns. If the 10G DTE XGXS is able to generate test patterns then the functionality is controlled using the transmit test-pattern enable bit in register 5.25.

45.2.5.8.3 Lane 3 sync (5.24.3)

When read as a one, bit 5.24.3 indicates that the XGXS receive lane 3 is synchronized. When read as a zero, bit 5.24.3 indicates that the XGXS receive lane 3 is not synchronized.

Table 45–103—10G DTE XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
5.24.15:13	Reserved	Ignore when read	RO
5.24.12	DTE XGXS lane alignment status	1 = DTE XGXS receive lanes aligned 0 = DTE XGXS receive lanes not aligned	RO
5.24.11	Pattern testing ability	1 = DTE XGXS is able to generate test patterns 0 = DTE XGXS is not able to generate test patterns	RO
5.24.10	Ignored	Value 0 or 1, writes ignored	RO
5.24.9:4	Reserved	Ignore when read	RO
5.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
5.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
5.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
5.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.5.8.4 Lane 2 sync (5.24.2)

When read as a one, bit 5.24.2 indicates that the XGXS receive lane 2 is synchronized. When read as a zero, bit 5.24.2 indicates that the XGXS receive lane 2 is not synchronized.

45.2.5.8.5 Lane 1 sync (5.24.1)

When read as a one, bit 5.24.1 indicates that the XGXS receive lane 1 is synchronized. When read as a zero, bit 5.24.1 indicates that the XGXS receive lane 1 is not synchronized.

45.2.5.8.6 Lane 0 sync (5.24.0)

When read as a one, bit 5.24.0 indicates that the XGXS receive lane 0 is synchronized. When read as a zero, bit 5.24.0 indicates that the XGXS receive lane 0 is not synchronized.

45.2.5.9 10G DTE XGXS test control register (Register 5.25)

The assignment of bits in the 10G DTE XGXS test control register is shown in Table 45–104. The default value for each bit of the 10G DTE XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.5.9.1 10G DTE XGXS test-pattern enable (5.25.2)

When bit 5.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 5.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10G

Table 45–104—10G DTE XGXS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
5.25.15:3	Reserved	Value always 0, writes ignored	R/W
5.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W
5.25.1:0	Test-pattern select	1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

DTE XGXS to generate test patterns is advertised by the pattern testing ability bit in register 5.24. A 10G DTE XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 5.25.2 is zero.

45.2.5.9.2 10G DTE XGXS test-pattern select (5.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 5.25.2 is selected using bits 5.25.1:0. When bits 5.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.6 TC registers

The assignment of registers in the TC MMD is shown in Table 45–105.

Table 45–105—TC registers

Register address	Register name
6.0	TC control
6.1	Reserved
6.2, 6.3	TC device identifier
6.4	TC speed ability
6.5, 6.6	TC devices in package
6.7 through 6.13	Reserved
6.14, 6.15	TC package identifier

Table 45–105—TC registers *(continued)*

Register address	Register name
6.16	10P/2B aggregation discovery control[a]
6.17	10P/2B aggregation and discovery status[a]
6.18, 6.19, 6.20	10P/2B aggregation discovery code[a]
6.21	10P/2B link partner PME aggregate control[a]
6.22, 6.23	10P/2B link partner PME aggregate data[a]
6.24	10P/2B TC CRC error counter
6.25, 6.26	10P/2B TPS-TC coding violations counter
6.27	10P/2B TC indications
6.28 through 6.32 767	Reserved
6.32 768 through 6.65 535	Vendor specific

[a]Register is defined only for -O port types and is reserved for -R ports

45.2.6.1 TC control register (Register 6.0)

The assignment of bits in the TC control register is shown in Table 45–106. The default value for each bit of the TC control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–106—TC control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.0.15	Reset	1 = TC reset 0 = Normal operation	R/W SC
6.0.14	Reserved	Value always 0, writes ignored	R/W
6.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
6.0.12:7	Reserved	Value always 0, writes ignored	R/W
6.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
6.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = Reserved	R/W
6.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.6.1.1 Reset (6.0.15)

Resetting a TC is accomplished by setting bit 6.0.15 to a one. This action shall set all TC registers to their default states. As a consequence, this action may change the internal state of the TC and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a TC shall return a value of one in bit 6.0.15 when a reset is in progress; otherwise, it shall return a value of zero. A TC is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 6.0.15. During a reset, a TC shall respond to reads from register bit 6.0.15.

NOTE—This operation may interrupt data communication. The data path of a TC, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset.

45.2.6.1.2 Speed selection (6.0.13, 6.0.6, 6.0.5:2)

Speed selection bits 6.0.13 and 6.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The operating mode of the TC may be selected using bits 5 through 2. The abilities of the TC are advertised in the TC speed ability register. A TC may ignore writes to the TC speed selection bits that select speeds it has not advertised in the TC speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The speed selection bits 6.0.5:2, when set to 0001, select the use of the 10PASS-TS and 2BASE-TL TC.

The TC speed selection defaults to a supported ability.

45.2.6.2 TC device identifier (Registers 6.2 and 6.3)

Registers 6.2 and 6.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of TC. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A TC may return a value of zero in each of the 32 bits of the TC device identifier.

The format of the TC device identifier is specified in 22.2.4.3.1.

45.2.6.3 TC speed ability (Register 6.4)

The assignment of bits in the TC speed ability register is shown in Table 45–107.

Table 45–107—TC speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
6.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
6.4.1	10PASS-TS/2BASE-TL capable	1 = TC is capable of operating as the 10P/2B TC 0 = TC is not capable of operating as the 10P/2B TC	RO
6.4.0	Reserved	Value always 0, writes ignored	RO

[a]RO = Read Only

45.2.6.3.1 10PASS-TS/2BASE-TL capable (6.4.1)

When read as a one, this bit indicates that the TC is able to operate as the 10PASS-TS/2BASE-TL TC, as specified in Clause 61.

45.2.6.4 TC devices in package registers (Registers 6.5, 6.6)

The TC devices in package registers are defined in Table 45–2.

45.2.6.5 TC package identifier registers (Registers 6.14, 6.15)

Registers 6.14 and 6.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the TC MMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A TC may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

45.2.6.6 10P/2B aggregation discovery control register (Register 6.16)

The 10P/2B aggregation discovery control register allows the STA of an -O port to determine the aggregation capabilities of an -R link-partner.

The 10P/2B aggregation discovery control register shall be implemented as a unique register for each TC MMD in a package. For example, a package implementing four PHYs would have four independent instances of the 10P/2B aggregation discovery control register, accessed by a read or write to each PHY.

For information on the encoding of this function on the physical link, see 61.4.7.

This register is defined for -O port subtypes only. The register bit definitions for the 10P/2B aggregation discovery control register are shown in Table 45–108.

Table 45–108—10P/2B aggregation discovery control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.16.15:2	Reserved	Value always 0, writes ignored	R/W
6.16.1:0	Discovery operation	01 = Ready (default) 00 = Set if clear 11 = Clear if same 10 = Get	R/W

[a]R/W = Read/Write

45.2.6.6.1 Discovery operation (6.16.1:0)

The Discovery operation bits are used to query and manipulate the remote discovery register. The remote discover register is not a Clause 45 object, but a variable of the PME aggregation PCS function on -R ports. The Discovery operation makes use of G.994.1 handshaking messages, therefore valid only when the link status is down (i.e., neither Initializing nor Up). Attempts to perform an operation while the link is Initializing or Up shall be ignored.

The default state of these bits is “Ready”. The bits shall indicate “Ready” any time the PME aggregation function is capable of performing an operation on the remote discovery register. If PAF is not supported, the discovery operation bits shall indicate “Ready” and ignore writes. These bits shall return to the “Ready” state upon MMD Reset.

If the STA sets the bits to "Get," the PME aggregation function queries the remote discovery register and returns its contents to the aggregation discovery code register.

If the STA sets the bits to "Set if clear," the PME aggregation function passes a message to the -R PCS instructing it to set the remote discovery register to the contents of the aggregation discovery code register, but only if the remote discovery register is all zeros.

If the STA sets the bits to "Clear if same," the PME aggregation function passes a message to the -R PCS instructing it to clear the remote discovery register, but only if the contents of the remote discovery register currently match the contents of the aggregation discovery code register.

While the requested operation is in progress, the PHY maintains the operation value in the bits. After the operation is complete, the PHY shall set the bits to indicate "Ready". If the operation does not complete within a 255 second time-out, the discovery operation result bit (6.17.0) will be set to "1" (operation unsuccessful), and the discovery operation bits will be set to "Ready".

45.2.6.7 10P/2B aggregation and discovery status register (Register 6.17)

The 10P/2B aggregation and discovery status register is defined for -O port subtypes only.

The assignment of bits in the 10P/2B aggregation and discovery status register is shown in Table 45–109.

Table 45–109—10P/2B aggregation and discovery status register bit definitions

Bit(s)	Name	Description	R/W[a]
6.17.15:2	Reserved	Value always 0, writes ignored	R/W
6.17.1	Link partner aggregate operation result	1 = operation unsuccessful 0 = operation completed successfully (default)	RO, LH
6.17.0	Discovery operation result	1 = operation unsuccessful 0 = discovery operation completed successfully (default)	RO, LH

[a]R/W = Read/Write, RO = Read Only, LH = Latches High

45.2.6.7.1 Link partner aggregate operation result (6.17.1)

When a link partner aggregate operation is complete, the PHY sets this bit to indicate the result of the operation. A "1" indicates that the operation could not be completed. This may be for a variety of reasons:

a) PMA/PMD link status is initializing or up.
b) The link partner is not present or not responding.

If PAF is not supported, this bit shall remain set to zero.

45.2.6.7.2 Discovery operation result (6.17.0)

When a discovery operation is complete, the PHY sets this bit to indicate the result of the operation. A "1" indicates that the operation could not be completed. This may be for a variety of reasons:

a) PMA/PMD link status is initializing or up.
b) A "Set if clear" operation was requested but the remote discovery register was not clear.
c) A "Clear if same" operation was requested but the remote discovery register did not match the aggregation discovery code register.
d) The link partner is not present or not responding.

If PAF is not supported, this bit shall read as zero.

45.2.6.8 10P/2B aggregation discovery code (Registers 6.18, 6.19, 6.20)

The 10P/2B aggregation discovery code registers store the value of the remote_discovery_register exchanged with the -R link partner.

This register is defined for -O port subtypes only.

These registers shall be implemented as unique registers for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the 10P/2B aggregation discovery code registers, accessed by a read or write to each PHY.

For information on the encoding of this function on the physical link, please see 61.4.7.

The assignment of bits for the 10P/2B aggregation discovery code registers are shown in Table 45–110.

Table 45–110—10P/2B aggregation discovery code bit definitions

Bit(s)	Name	Description	R/W[a]
6.18.15:0	Code [47:32]	The two most significant octets of the aggregation discovery code	R/W
6.19.15:0	Code [31:16]	The two middle octets of the aggregation discovery code	R/W
6.20.15:0	Code [15:0]	The two least significant octets of the aggregation discovery code	R/W

[a]R/W = Read/Write

45.2.6.9 10P/2B link partner PME aggregate control register (Register 6.21)

The 10P/2B link partner PME aggregate control register allows the STA of an -O port to read and write the remote PME_Aggregate_register (see 61.2.2.8.3).

The 10P/2B link partner PME aggregate control register shall be implemented as a unique register for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the 10P/2B link partner PME aggregate control register, accessed by a read or write to each PHY.

This register is defined for -O port subtypes only.

The register bit definitions for the 10P/2B link partner PME aggregate control register are shown in Table 45–111.

Table 45–111—10P/2B link partner PME aggregate control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.21.15:2	Reserved	Value always 0, writes ignored	R/W
6.21.1:0	Link partner aggregate operation	01 = Ready (default) 00 = Set 11 = invalid 10 = Get	R/W

[a]R/W = Read/Write

45.2.6.9.1 Link partner aggregate operation (1.21.1:0)

The Link partner aggregate operation bits are used to query and manipulate the remote PME_Aggregate_register. This operation makes use of G.994.1 handshaking messages and therefore must be performed only when the link status is down (i.e., neither Initializing nor Up). Attempts to perform an operation while the link is Initializing or Up shall be ignored.

The default state of these bits is "Ready." The bits shall indicate "Ready" any time the PME aggregation function is capable of performing an operation on the remote PME_Aggregate_register. If PAF is not supported, the link partner aggregate operation bits shall indicate "Ready" ignore writes. These bits shall return to the "Ready" state upon MMD Reset.

If the STA sets the bits to "Get," the PME aggregation function queries the remote PME_Aggregate_register and returns its contents to the 10P/2B link partner PME aggregate data register (see 45.2.6.10).

If the STA sets the bits to "Set," the PME aggregation function passes a message to the -R PCS instructing it to set the bit location in the remote PME_Aggregate_register corresponding to the TC on which the message was received to the contents of bit 0 of the 10P/2B link partner PME aggregate data register.

While the requested operation is in progress, the PHY maintains the operation value in the bits. After the operation is complete, the PHY shall set the bits to indicate "Ready".

45.2.6.10 10P/2B link partner PME aggregate data (Registers 6.22, 6.23)

The 10P/2B link partner PME aggregate data registers store the data for the link partner aggregate operation. This register either contains the result of a "Get" operation, the data sent in a "Set" operation, or all zeros following an MMD reset.

These registers are defined for -O port subtypes only.

These registers shall be implemented as unique registers for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the registers, accessed by a read or write to each PHY.

The assignment of bits for the 10P/2B link partner PME aggregate data registers are shown in Table 45–112.

Table 45–112—10P/2B link partner PME aggregate data registers bit definitions

Bit(s)	Name	Description	R/W[a]
6.22.15:0	Data[31:16]	The two most significant octets of the link partner PME aggregate data	R/W
6.23.15:0	Data[15:0]	The two least significant octets of the link partner PME aggregate data	R/W

[a]R/W = Read/Write

45.2.6.11 10P/2B TC CRC error register (Register 6.24)

The 10P/2B TC CRC error register is a 16 bit counter that contains the number of TC frames received with the TC_CRC_error primitive asserted, defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B TC CRC error register are shown in Table 45–113.

Table 45–113—10P/2B TC CRC error register bit definitions

Bit(s)	Name	Description	R/W[a]
6.24.15:0	CRC errors[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.6.12 10P/2B TPS-TC coding violations counter (Registers 6.25, 6.26)

The 10P/2B TPS-TC coding violations counter is a 32-bit counter that contains the number of 64/64-octet encapsulation errors, defined in 61.3.3.1. This counter increments for each 64/65-octet received with the TC_coding_error signal asserted. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B TPS-TC coding violations counter are shown in Table 45–114.

Table 45–114—10P/2B TPS-TC coding violations counter bit definitions

Bit(s)	Name	Description	R/W[a]
6.25.15:0	Coding violations[31:16]	The high order bytes of the counter	RO, MW
6.26.15:0	Coding violations[15:0]	The low order bytes of the counter	RO, MW

[a]RO = Read Only, MW = Multi-word

45.2.6.13 10P/2B TC indications register (Register 6.27)

The 10P/2B TC indications register reflects the state of the TC sync detect state machine and the state of the link partner TC sync detect state machine (if present) (see 61.3.3.5). The assignment of bits in the 10P/2B TC indications register is shown in Table 45–115.

Table 45–115—10P/2B TC indications register bit definitions

Bit(s)	Name	Description	R/W[a]
6.27.15:9	Reserved	Value always 0	RO
6.27.8	Local TC synchronized	1 = TC_synchronized is TRUE 0 = TC_synchronized is FALSE	RO
6.27.7:1	Reserved	Value always 0	RO
6.27.0	Remote TC synchronized	1 = remote_TC_out_of_sync is FALSE 0 = remote_TC_out_of_sync is TRUE	RO

[a]RO = Read Only

45.2.6.13.1 Local TC synchronized (6.27.8)

This bit is read as a one when the TC_synchronized variable in the TC sync detect state machine is TRUE (see 61.2.3.3.8). In all other cases, this bit is read as zero.

45.2.6.13.2 Remote TC synchronized (6.27.0)

This bit is read as a one when the remote_TC_out_of_sync variable in the link partner TC sync detect state machine is FALSE (see 61.2.3.3.8). In all other cases, this bit is read as zero.

45.2.7 Clause 22 extension registers

As new management features are added to 10, 100 and 1000 Mb/s PHYs, more register space is required beyond that defined in Clause 22. The Clause 22 extension MMD provides this space. This MMD is defined only for 10, 100, 1000 Mb/s PHYs. Since these PHYs do not segment their management by their sublayers, all management extensions to these PHYs will appear in the Clause 22 extension MMD.

The assignment of registers in the Clause 22 extension MMD is shown in Table 45–116.

Table 45–116—Clause 22 extension registers

Register address	Register name
29.0 through 29.4	Reserved
29.5, 29.6	Clause 22 extension devices in package
29.7	FEC capability
29.8	FEC control
29.9	FEC buffer head coding violation counter
29.10	FEC corrected blocks counter
29.11	FEC uncorrected blocks counter
29.12 through 29.32 767	Reserved

45.2.7.1 Clause 22 extension devices in package registers (Registers 29.5, 29.6)

The Clause 22 extension devices in package registers are defined in Table 45–7.

45.2.7.2 FEC capability register (Register 29.7)

The assignment of bits in the FEC capability register is shown in Table 45–117.

Table 45–117—FEC capability register bit definitions

Bit(s)	Name	Description	R/W[a]
29.7.15:1	Reserved	Value always 0, writes ignored	RO
29.7.0	FEC capable	1 = FEC supported 0 = FEC unsupported	RO

[a]RO = Read Only

45.2.7.2.1 FEC capable (29.7.0)

When read as a one, this bit indicates that the PHY supports forward error correction. When read as a zero, the PHY does not support forward error correction.

45.2.7.3 FEC control register (Register 29.8)

The assignment of bits in the FEC control register is shown in Table 45–118.

Table 45–118—FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
29.8.15:1	Reserved	Value always 0, writes ignored	R/W
29.8.0	FEC enable	1 = FEC enabled 0 = FEC disabled	R/W

[a]R/W = Read/Write

45.2.7.3.1 FEC enable (29.8.0)

When written as a one, this bit enables the PHY's forward error correction. When written as a zero, FEC is disabled. This bit shall be set to zero upon execution of a PHY reset.

45.2.7.4 FEC buffer head coding violation counter (Register 29.9)

The assignment of bits in the FEC buffer head coding violation counter register is shown in Table 45–119. See 65.2.3.6.1 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–119—FEC buffer head coding violation counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.9.15:0	FEC buffer head coding violation counter	Error counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.7.5 FEC corrected blocks counter (Register 29.10)

The assignment of bits in the FEC corrected blocks counter register is shown in Table 45–120. See 65.2.3.6.2 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–120—FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.10.15:0	FEC corrected blocks counter	Error counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.7.6 FEC uncorrected blocks counter (Register 29.11)

The assignment of bits in the FEC uncorrected blocks counter register is shown in Table 45–121. See 65.2.3.6.3 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–121—FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.11.15:0	FEC uncorrected blocks counter	Error counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.8 Vendor specific MMD 1 registers

The assignment of registers in the vendor specific MMD 1 is shown in Table 45–122. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

Table 45–122—Vendor specific MMD 1 registers

Register address	Register name
30.0, 30.1	Vendor specific
30.2, 30.3	Vendor specific MMD 1 device identifier
30.4 through 30.7	Vendor specific
30.8	Vendor specific MMD 1 status register
30.9 through 30.13	Vendor specific
30.14, 30.15	Vendor specific MMD 1 package identifier
30.16 through 30.65 535	Vendor specific

45.2.8.1 Vendor specific MMD 1 device identifier (Registers 30.2 and 30.3)

Registers 30.2 and 30.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 1 device identifier.

The format of the vendor specific MMD 1 device identifier is specified in 22.2.4.3.1.

45.2.8.2 Vendor specific MMD 1 status register (Register 30.8)

The assignment of bits in the vendor specific MMD 1 status register is shown in Table 45–123. All the bits in the vendor specific MMD 1 status register are read only; a write to the vendor specific MMD 1 status register shall have no effect.

Table 45–123—Vendor specific MMD 1 status register bit definitions

Bit(s)	Name	Description	R/W[a]
30.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
30.8.13:0	Reserved	Ignore when read	RO

[a]RO = Read Only

45.2.8.2.1 Device present (30.8.15:14)

When read as <10>, bits 30.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 30.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.8.3 Vendor specific MMD 1 package identifier (Registers 30.14 and 30.15)

Registers 30.14 and 30.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD 1 is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD 1 may return a value of zero in each of the 32 bits of the vendor specific MMD 1 package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 1 package identifier is specified in 22.2.4.3.1.

45.2.9 Vendor specific MMD 2 registers

The assignment of registers in the vendor specific MMD 2 is shown in Table 45–124. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

45.2.9.1 Vendor specific MMD 2 device identifier (Registers 31.2 and 31.3)

Registers 31.2 and 31.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 2 device identifier.

Table 45–124—Vendor specific MMD 2 registers

Register address	Register name
31.0, 31.1	Vendor specific
31.2, 31.3	Vendor specific MMD 2 device identifier
31.4 through 31.7	Vendor specific
31.8	Vendor specific MMD 2 status register
31.9 through 31.13	Vendor specific
31.14, 30.15	Vendor specific MMD 2 package identifier
31.16 through 31.65 535	Vendor specific

The format of the vendor specific MMD 2 device identifier is specified in 22.2.4.3.1.

45.2.9.2 Vendor specific MMD 2 status register (Register 31.8)

The assignment of bits in the vendor specific MMD 2 status register is shown in Table 45–125. All the bits in the vendor specific MMD 2 status register are read only; a write to the vendor specific MMD status register shall have no effect.

Table 45–125—Vendor specific MMD 2 status register bit definitions

Bit(s)	Name	Description	R/W[a]
31.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
31.8.13:0	Reserved	Ignore when read	RO

[a]RO = Read Only

45.2.9.2.1 Device present (31.8.15:14)

When read as <10>, bits 31.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 31.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.9.3 Vendor specific MMD 2 package identifier (Registers 31.14 and 31.15)

Registers 31.14 and 31.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 2 package identifier is specified in 22.2.4.3.1.

45.3 Management frame structure

The MDIO interface frame structure is compatible with the one defined in 22.2.4.5 such that the two systems can co-exist on the same MDIO bus. The electrical specification for the MDIO interface is incompatible to that defined in 22.2.4.5; therefore, if the two systems are to co-exist on the same bus, a voltage translation device is required (see Annex 45A). The extensions that are used for MDIO indirect register accesses are specified in Table 45–126.

Table 45–126—Extensions to management frame format for indirect access

	Management frame fields							
Frame	**PRE**	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**ADDRESS / DATA**	**IDLE**
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

Each MMD shall implement a sixteen bit address register that stores the address of the register to be accessed by data transaction frames. The address register shall be overwritten by address frames. At power up or device reset, the contents of the address register are undefined.

Write, read, and post-read-increment-address frames shall access the register whose address is stored in the address register. Write and read frames shall not modify the contents of the address register.

Upon receiving a post-read-increment-address frame and having completed the read operation, the MMD shall increment the address register by one. For the case where the MMD's address register contains 65 535, the MMD shall not increment the address register.

Implementations that incorporate several MMDs within a single component shall implement separate address registers so that the MMD's address registers operate independently of one another.

45.3.1 IDLE (idle condition)

The idle condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the MMD's pull-up resistor will pull the MDIO line to a one.

45.3.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC to provide the MMD with a pattern that it can use

to establish synchronization. An MMD shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

45.3.3 ST (start of frame)

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 shall be ignored by the devices specified in Clause 45.

45.3.4 OP (operation code)

The operation code field indicates the type of transaction being performed by the frame. A <00> pattern indicates that the frame payload contains the address of the register to access. A <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address frame. A <11> pattern indicates that the frame is read operation. A <10> pattern indicates that the frame is a post-read-increment-address operation.

45.3.5 PRTAD (port address)

The port address is five bits, allowing 32 unique port addresses. The first port address bit to be transmitted and received is the MSB of the address. A station management entity must have a priori knowledge of the appropriate port address for each port to which it is attached, whether connected to a single port or to multiple ports.

45.3.6 DEVAD (device address)

The device address is five bits, allowing 32 unique MMDs per port. The first device address bit transmitted and received is the MSB of the address.

45.3.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the device address field and the data field of a management frame to avoid contention during a read transaction. For a read or post-read-increment-address transaction, both the STA and the MMD shall remain in a high-impedance state for the first bit time of the turnaround. The MMD shall drive a zero bit during the second bit time of the turnaround of a read or post-read-increment-address transaction. During a write or address transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22–13 shows the behavior of the MDIO signal during the turnaround field of a read or post-read-increment-address transaction.

45.3.8 ADDRESS / DATA

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register. For a read or post-read-increment-address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

45.4 Electrical interface

45.4.1 Electrical specification

The electrical characteristics of the MDIO interface are shown in Table 45–127. The MDIO uses signal levels that are compatible with devices operating at a nominal supply voltage of 1.2 V. More information on the

electrical interface is given in Annex 45A. Voltage translators between the Clause 22 electrical interface and the Clause 45 electrical interface are described in 45A.3 and 45A.4.

NOTE—It is possible to implement the MDIO electrical interface using open drain buffers and a resistive pull-up to a V_{DD} of 1.2 V (see 45A.1).

Table 45–127—MDIO electrical interface characteristics

Symbol	Parameter	Condition	Min.	Max.
V_{IH}	Input high voltage		0.84 V	1.5 V
V_{IL}	Input low voltage		–0.3 V	0.36 V
V_{OH}	Output high voltage	I_{OH} = -100 uA	1.0 V	1.5 V
V_{OL}	Output low voltage	I_{OL} = 100 uA	–0.3 V	0.2 V
I_{OH}[a]	Output high current	V_{OH} = 1.0 V		–4 mA
I_{OL}	Output low current	V_{OL} = 0.2 V	+4 mA	
C_i	Input capacitance			10 pF
C_L	Total capacitive load			470 pF

[a]I_{OH} parameter is not applicable to open drain drivers.

45.4.2 Timing specification

MDIO is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the MMD. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 45–3, measured at the MMD.

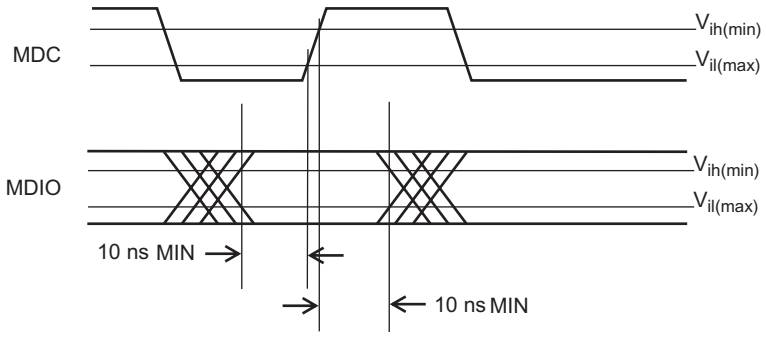

Figure 45–3—MDIO sourced by STA

When the MDIO signal is sourced by the MMD, it is sampled by the STA synchronously with respect to the beginning of the rising edge of MDC. The clock to output delay from the MMD, as measured at the STA, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 45–4.

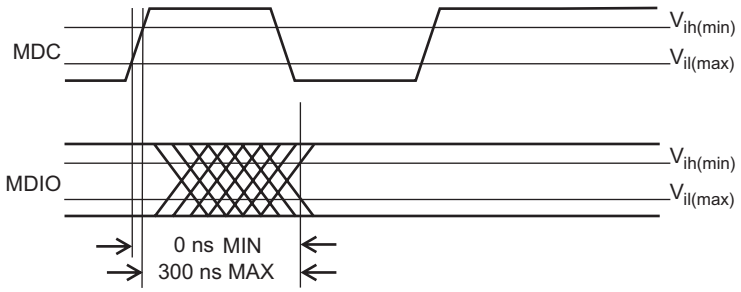

Figure 45–4—MDIO sourced by MMD

The timing specification for the MDC signal is given in 22.2.2.11.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface[1]

45.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 45, MDIO interface, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

45.5.2 Identification

45.5.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

45.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2005, Clause 45, Management Data Input/Output (MDIO) Interface
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2005.)	

Date of Statement	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA	Implementation of PMA/PMD MMD	45.2.1		O	Yes [ ] No [ ]
*WIS	Implementation of WIS MMD	45.2.2		O	Yes [ ] No [ ]
*PCS	Implementation of PCS MMD	45.2.3		O	Yes [ ] No [ ]
*PX	Implementation of PHY XS MMD	45.2.4		O	Yes [ ] No [ ]
*DX	Implementation of DTE XS MMD	45.2.5		O	Yes [ ] No [ ]
*VSA	Implementation of Vendor Specific MMD 1	45.2.8		O	Yes [ ] No [ ]
*VSB	Implementation of Vendor Specific MMD 2	45.2.9		O	Yes [ ] No [ ]
*TC	Implementation of the TC MMD	45.2.6		10P*2B:M	Yes [ ] No [ ]
*CTT	Implementation of the Clause 22 extension MMD	45.2.7		O	Yes [ ] No [ ]
*ODB	Open drain buffer	45.4.1		O	Yes [ ] No [ ]

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.3.1 MDIO signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SF1	MDIO uses three-state drivers	45.4.1		M	Yes [ ]

45.5.3.2 PMA/PMD MMD options

Item	Feature	Subclause	Value/Comment	Status	Support
*ALB	Implementation of PMA loop-back function	45.2.1.1.4		PMA:O	Yes [ ] No [ ] N/A [ ]
*PLF	Implementation of fault detection	45.2.1.7		PMA:O	Yes [ ] No [ ] N/A [ ]
*PTD	Implementation of transmit disable function	45.2.1.8		PMA:O	Yes [ ] No [ ] N/A [ ]
*10P	Implementation of the 10PASS-TS PMA/PMD	45.2.1.4		O	Yes [ ] No [ ]
*2B	Implementation of the 2BASE-TL PMA/PMD	45.2.1.4		O	Yes [ ] No [ ]

45.5.3.3 PMA/PMD management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MM1	Device responds to all register addresses for that device	45.2		PMA:M	Yes [ ] N/A [ ]
MM2	Writes to undefined and read-only registers have no effect	45.2		PMA:M	Yes [ ] N/A [ ]
MM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		PMA:M	Yes [ ] N/A [ ]
MM4	Reserved and unsupported bits return a value of zero	45.2		PMA:M	Yes [ ] N/A [ ]
MM5	Latching low bits remain low until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM7	Latching high bits remain high until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM9	Action on reset	45.2.1.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PMA:M	Yes [ ] N/A [ ]
MM10	Return 1 until reset completed	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM11	Control and management interfaces are restored to operation within 0.5 s of reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM12	Responds to reads of bit 15 and 1.8.15:14 during reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM13	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.1.1.2		PMA:M	Yes [ ] N/A [ ]
MM14	Speed selection bits 13 and 6 are written as one	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM15	Invalid writes to speed selection bits are ignored	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM16	PMA is set into loopback mode when bit 0 is set to a one	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM17	PMA transmit data is returned on receive path when in loopback	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]
MM18	PMA ignores writes to this bit if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM19	PMA returns a value of zero when read if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM20	Writes to status 1 register have no effect	45.2.1.2		PMA:M	Yes [ ] N/A [ ]
MM21	Receive link status implemented with latching low behavior	45.2.1.2.2		PMA:M	Yes [ ] N/A [ ]
MM22	Unique identifier is composed of OUI, model number and revision	45.2.1.3		PMA:M	Yes [ ] N/A [ ]
MM23	10G PMA/PMD type is selected using bits 2:0	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM24	10G PMA/PMD ignores writes to type selection bits that select types that it has not advertised	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM25	Writes to the status 2 register have no effect	45.2.1.7		PMA:M	Yes [ ] N/A [ ]
MM26	PMA/PMD returns a value of zero for transmit fault if it is unable to detect a transmit fault	45.2.1.7.4		PMA:M	Yes [ ] N/A [ ]
MM27	Transmit fault is implemented using latching high behavior	45.2.1.7.4		PMA*PLF:M	Yes [ ] N/A [ ]
MM28	PMA/PMD returns a value of zero for receive fault if it is unable to detect a receive fault	45.2.1.7.5		PMA*!PLF:M	Yes [ ] N/A [ ]
MM29	Receive fault is implemented using latching high behavior	45.2.1.7.5		PMA*PLF:M	Yes [ ] N/A [ ]
MM30	Writes to register 9 are ignored by device that does not implement transmit disable	45.2.1.8		PMA*!PTD:M	Yes [ ] N/A [ ]
MM31	Single wavelength device uses bit 1.9.0 for transmit disable	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM32	Single wavelength device ignores writes to bits 1 – 4 and returns a value of zero for them	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM33	Setting bit 4 to a one disables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM34	Setting bit 4 to a zero enables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM35	Setting bit 3 to a one disables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM36	Setting bit 3 to a zero enables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM37	Setting bit 2 to a one disables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM38	Setting bit 2 to a zero enables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM39	Setting bit 1 to a one disables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM40	Setting bit 1 to a zero enables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM41	Setting bit 0 to a one disables transmission	45.2.1.8.5		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM42	Setting bit 0 to a zero enables transmission	45.2.1.8.5	Only if all lane transmit disables are zero	PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM43a	Writes to the extended ability register have no effect	45.2.1.10		PMA:M	Yes [ ] N/A [ ]
MM43b	Unique identifier is composed of OUI, model number and revision	45.2.1.11		PMA:M	Yes [ ] N/A [ ]
MM46	Bit indicates link down while initializing	45.2.1.2.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM47	Bit remains a one and writing a one is ignored when link is up or initializing	45.2.1.11		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM48	Bit set to zero upon reset or upon link down	45.2.1.12.1	-O subtypes only	PMA*10P*2B:M	Yes [ ] N/A [ ]
MM49	Bit set to one upon reset or upon link down	45.2.1.12.1	-R subtypes only	PMA*10P*2B:M	Yes [ ] N/A [ ]
MM50	Handshake tones not sent while bit is set to zero	45.2.1.12.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM51	Writes to set unsupported modes or when link is not down are ignored	45.2.1.12.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM52	Setting bit to one to one issues a cleardown command	45.2.1.12.5		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM53	MMD clears bit to zero when cleardown command is issued or on reset	45.2.1.12.5		PMA*10P*2B:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM54	Writes ignored if link is not in "Link down (ready)" state	45.2.1.12.5	Link state described in 45.2.1.13.4	PMA*10P*2B:M	Yes [ ] N/A [ ]
MM55	PMA/PMD does not respond to handshake tones while bit is set to one	45.2.1.12.6		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM56	PMA/PMD responds to handshake tones properly when bit is set to zero	45.2.1.12.6		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM57	Bit set to zero upon MMD reset	45.2.1.12.6		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM58	Writes to set unsupported modes are ignored	45.2.1.12.7		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM59	Bits zero when link is down or initializing	45.2.1.13.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM60	Bits set indicate linked port type or link status	45.2.1.13.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM61	Bits indicate 001 while link is initializing	45.2.1.13.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM62	Bits indicate 000 when link is down and handshake tones are not detected	45.2.1.13.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM63	Bits indicate 100 when link is down and handshake tones are detected	45.2.1.13.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM64	Bit held as one during operation, clears to zero after	45.2.1.14.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM65	Result = failed after 10 second timeout	45.2.1.14.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM66	Writes to one while link is down are marked completed and failed	45.2.1.14.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM67	Bit held as one during operation, clears to zero after	45.2.1.14.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM68	Result = failed after 10 second timeout	45.2.1.14.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM69	Writes to one while link is down are marked completed and failed	45.2.1.14.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM70	Bit set to result of the "Get" operation	45.2.1.15.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM71	Bit set to zero on read or reset	45.2.1.15.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM72	Bit set to result of the "Send" operation	45.2.1.15.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM73	Bits are reset to zero when read or on reset	45.2.1.16		PMA*10P*2B:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM74	Bits are held to all ones upon counter overflow	45.2.1.16		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM75	Bits are reset to zero when read or reset	45.2.1.23		PMA*10P:M	Yes [ ] N/A [ ]
MM76	Bits are reset to zero when read or reset	45.2.1.24		PMA*10P:M	Yes [ ] N/A [ ]
MM77	Bits are held at all ones when PHY cannot determine value	45.2.1.27.1	ex: While link is down	PMA*10P:M	Yes [ ] N/A [ ]
MM78	Bit remain as one while tones are being refreshed	45.2.1.37.1		PMA*10P:M	Yes [ ] N/A [ ]
MM79	Bit set to zero when operation completes or upon reset	45.2.1.37.1		PMA*10P:M	Yes [ ] N/A [ ]
MM80	Bit remain as one while tones are being activated/deactivated	45.2.1.37.2		PMA*10P:M	Yes [ ] N/A [ ]
MM81	Bit set to zero when operation completes or upon reset	45.2.1.37.2		PMA*10P:M	Yes [ ] N/A [ ]
MM82	Bit remain as one while tone direction is being changed	45.2.1.37.3		PMA*10P:M	Yes [ ] N/A [ ]
MM83	Bit set to zero when operation completes or upon reset	45.2.1.37.3		PMA*10P:M	Yes [ ] N/A [ ]
MM84	Bit remain as one while SNR margins parameters are loaded	45.2.1.37.4		PMA*10P:M	Yes [ ] N/A [ ]
MM85	Bit set to zero when operation completes or upon reset	45.2.1.37.4		PMA*10P:M	Yes [ ] N/A [ ]
MM86	Bit remain as one while PSD level is set	45.2.1.37.5		PMA*10P:M	Yes [ ] N/A [ ]
MM87	Bit set to zero when operation completes or upon reset	45.2.1.37.5		PMA*10P:M	Yes [ ] N/A [ ]
MM88	Bit remain as one while reference PSD level is set	45.2.1.37.6		PMA*10P:M	Yes [ ] N/A [ ]
MM89	Bit set to zero when operation completes or upon reset	45.2.1.37.6		PMA*10P:M	Yes [ ] N/A [ ]
MM90	Bits are reset to zero when read or upon reset	45.2.1.38.1		PMA*10P:M	Yes [ ] N/A [ ]
MM91	Bits read as zero	45.2.1.39.6		PMA*10P:M	Yes [ ] N/A [ ]
MM92	Bits read as zero	45.2.1.39.7		PMA*10P:M	Yes [ ] N/A [ ]
MM93	Writes to an invalid value are ignored	45.2.1.41	Valid values are decimal 10, 20, or 40	PMA*10P:M	Yes [ ] N/A [ ]
MM94	Bits set to default value on MMD reset	45.2.1.41	Default value is decimal 20	PMA*10P:M	Yes [ ] N/A [ ]
MM95	Writes to set an invalid value are ignored	45.2.1.44.1	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM96	Writes to set an invalid value are ignored	45.2.1.44.2	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM97	Writes to set an invalid value are ignored	45.2.1.44.3	Valid values are decimal 1through 86	PMA*10P:M	Yes [ ] N/A [ ]
MM98	Writes to set an invalid value are ignored	45.2.1.44.5	Invalid value is 11	PMA*10P:M	Yes [ ] N/A [ ]
MM99	Bits set to zero when read or reset	45.2.1.45		PMA*2B:M	Yes [ ] N/A [ ]
MM100	Bits set to zero when read or reset	45.2.1.47		PMA*2B:M	Yes [ ] N/A [ ]
MM101	Bits set to zero when read or reset	45.2.1.49		PMA*2B:M	Yes [ ] N/A [ ]
MM102	Bits set to zero when read or reset	45.2.1.51		PMA*2B:M	Yes [ ] N/A [ ]
MM103	Bits set to zero when read or reset	45.2.1.53		PMA*2B:M	Yes [ ] N/A [ ]
MM104	Writes to set an invalid value are ignored	45.2.1.58.1	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM105	Writes to set an invalid value are ignored	45.2.1.58.2	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM106	Writes to set an invalid value are ignored	45.2.1.58.3	Valid values are decimal 1through 86	PMA*10P:M	Yes [ ] N/A [ ]
MM107	Writes to set an invalid value are ignored	45.2.1.58.5	Invalid value is 11	PMA*10P:M	Yes [ ] N/A [ ]

45.5.3.4 WIS options

Item	Feature	Subclause	Value/Comment	Status	Support
*WPT	Implementation of PRBS31 pattern testing	45.2.2		WIS:O	Yes [ ] No [ ] N/A [ ]

45.5.3.5 WIS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
WM1	Device responds to all register addresses for that device	45.2		WIS:M	Yes [ ] N/A [ ]
WM2	Writes to undefined and read-only registers have no effect	45.2		WIS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
WM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		WIS:M	Yes [ ] N/A [ ]
WM4	Reserved and unsupported bits return a value of zero	45.2		WIS:M	Yes [ ] N/A [ ]
WM5	Latching low bits remain low until after they have been read via the management interface	45.2		WIS:M	Yes [ ] N/A [ ]
WM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ ] N/A [ ]
WM7	Latching high bits remain high until after they have been read via the management interface	45.2		WIS:M	Yes [ ] N/A [ ]
WM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ ] N/A [ ]
WM9	Action on reset	45.2.2.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	WIS:M	Yes [ ] N/A [ ]
WM10	Return 1 until reset completed	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM11	Reset completes within 0.5 s	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM12	Responds to reads of bits 2.0.15 and 2.8.15:14 during reset	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM13	Loopback mode	45.2.2.1.2	Whenever bit 2.0.14 is set to a one	WIS:M	Yes [ ] N/A [ ]
WM14	Data received from PMA ignored during loopback	45.2.2.1.2		WIS:M	Yes [ ] N/A [ ]
WM15	Transmit data returned on receive path during loopback	45.2.2.1.2		WIS:M	Yes [ ] N/A [ ]
WM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.2.1.3		WIS:M	Yes [ ] N/A [ ]
WM17	Speed selection bits 13 and 6 are written as one	45.2.2.1.4		WIS:M	Yes [ ] N/A [ ]
WM18	Invalid writes to speed selection bits are ignored	45.2.2.1.4		WIS:M	Yes [ ] N/A [ ]
WM19	Writes to status 1 register have no effect	45.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM20	Fault bit implemented using latching high behavior	45.2.2.2.1		WIS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
WM21	Link status bit implemented using latching low behavior	45.2.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM22	Unique identifier is composed of OUI, model number and revision	45.2.2.3		WIS:M	Yes [ ] N/A [ ]
WM23	Setting bit 2.7.5 to a one enables PRBS31 receive pattern testing if bit 2.8.1 is a one and bit 2.7.2 is not a one	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM24	Setting bit 2.7.5 to a zero disables PRBS31 receive pattern testing	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM25	Setting bit 2.7.4 to a one enables PRBS31 transmit pattern testing if bit 2.8.1 is a one and bit 2.7.1 is not a one	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM26	Setting bit 2.7.4 to a zero disables PRBS31 transmit pattern testing	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM27	Setting bit 3 to one selects the square wave test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM28	Setting bit 3 to zero selects the pseudo random test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM29	Setting bit 2 to one enables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM30	Setting bit 2 to zero disables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM31	Setting bit 1 to one enables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM32	Setting bit 1 to zero disables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM33	Setting bit 0 to a one enables 10GBASE-W logic and sets interface speed	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM34	Setting bit 0 to a zero disables 10GBASE-W logic, sets interface speed. and bypasses data	45.2.2.6.6		WIS:O	Yes [ ] N/A [ ]
WM35	Writes to bit are ignored by WIS not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM36	Bit returns one when read if WIS is not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM37	Writes to status 2 register have no effect	45.2.2.7		WIS:M	Yes [ ] N/A [ ]
WM38	Counter is reset to all zeros when read or reset	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
WM39	Counter is held at all ones at overflow	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]
WM40	Unique identifier is composed of OUI, model number and revision	45.2.2.9		WIS:M	Yes [ ] N/A [ ]
WM41	Writes to Status 3 register have no effect	45.2.2.10		WIS:M	Yes [ ] N/A [ ]
WM42	SEF bit implemented using latching high behavior	45.2.2.10.1		WIS:M	Yes [ ] N/A [ ]
WM43	Far end PLM-P/LCD-P bit implemented using latching high behavior	45.2.2.10.2		WIS:M	Yes [ ] N/A [ ]
WM44	Far end AIS-P/LOP-P bit implemented using latching high behavior	45.2.2.10.3		WIS:M	Yes [ ] N/A [ ]
WM45	LOF bit implemented using latching high behavior	45.2.2.10.4		WIS:M	Yes [ ] N/A [ ]
WM46	LOS bit implemented using latching high behavior	45.2.2.10.5		WIS:M	Yes [ ] N/A [ ]
WM47	RDI-L bit implemented using latching high behavior	45.2.2.10.6		WIS:M	Yes [ ] N/A [ ]
WM48	AIS-L bit implemented using latching high behavior	45.2.2.10.7		WIS:M	Yes [ ] N/A [ ]
WM49	LCD-P bit implemented using latching high behavior	45.2.2.10.8		WIS:M	Yes [ ] N/A [ ]
WM50	PLM-P bit implemented using latching high behavior	45.2.2.10.9		WIS:M	Yes [ ] N/A [ ]
WM51	AIS-P bit implemented using latching high behavior	45.2.2.10.10		WIS:M	Yes [ ] N/A [ ]
WM52	LOP-P bit implemented using latching high behavior	45.2.2.10.11		WIS:M	Yes [ ] N/A [ ]

45.5.3.6 PCS options

Item	Feature	Subclause	Value/Comment	Status	Support
*CR	Implementation of 10GBASE-R PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*CX	Implementation of 10GBASE-X PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*XP	Implementation of 10GBASE-X pattern testing	45.2.3		PCS* CX:O	Yes [ ] No [ ] N/A [ ]
*PPT	Implementation of PRBS31 pattern testing	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*EPC	Implementation of the 10BASE-TS/2BASE-TL PCS	45.2.3.17		PCS:O	Yes [ ] No [ ] N/A [ ]
*PAF	Implementation of the PME aggregation function	45.2.3.17		PCS*EPC:O	Yes [ ] No [ ] N/A [ ]

45.5.3.7 PCS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Device responds to all register addresses for that device	45.2		PCS:M	Yes [ ] N/A [ ]
RM2	Writes to undefined and read-only registers have no effect	45.2		PCS:M	Yes [ ] N/A [ ]
RM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PCS:M	Yes [ ] N/A [ ]
RM4	Reserved and unsupported bits return a value of zero	45.2		PCS:M	Yes [ ] N/A [ ]
RM5	Latching low bits remain low until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]
RM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM7	Latching high bits remain high until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]
RM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM9	Action on reset	45.2.3.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PCS:M	Yes [ ] N/A [ ]
RM10	Return 1 until reset completed	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM11	Reset completes within 0.5 s	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM12	Device responds to reads of register bits 3.0.15 and 3.5.15:14 during reset	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM13	Loopback mode	45.2.3.1.2	Whenever bit 3.0.14 is set to a one	PCS:M	Yes [ ] N/A [ ]
RM14	Transmit data is returned on the receive path during loopback	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM15	Writes to loopback bit are ignored when operating at 10 Gb/s with port type selections other than 10GBASE-R	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM16	Loopback bit returns zero when operating at 10 Gb/s with port type selections other than 10GBASE-R	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM17	Device responds to transactions necessary to exit low-power mode while in low- power state	45.2.3.1.3		PCS:M	Yes [ ] N/A [ ]
RM18	Speed selection bits 13 and 6 are written as one	45.2.3.1.4		PCS:M	Yes [ ] N/A [ ]
RM19	Invalid writes to speed selection bits are ignored	45.2.3.1.4		PCS:M	Yes [ ] N/A [ ]
RM20	Writes to PCS status 1 register have no effect	45.2.3.2		PCS:M	Yes [ ] N/A [ ]
RM21	Receive link status implemented using latching low behavior	45.2.3.2.2		PCS:M	Yes [ ] N/A [ ]
RM22	Unique identifier is composed of OUI, model number and revision	45.2.3.3		PCS:M	Yes [ ] N/A [ ]
RM23	PCS type is selected using bits 1 through 0	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
RM24	Writes to the type selection bits that select types that have not been advertised are ignored	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
RM25	Writes to PCS status 2 register have no effect	45.2.3.7		PCS:M	Yes [ ] N/A [ ]
RM26	Transmit fault implemented with latching high behavior	45.2.3.7.2		PCS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM27	Receive fault implemented with latching high behavior	45.2.3.7.3		PCS:M	Yes [ ] N/A [ ]
RM28	Unique identifier is composed of OUI, model number and revision	45.2.3.8		PCS:M	Yes [ ] N/A [ ]
RM29	Writes to 10GBASE-X PCS status register have no effect	45.2.3.9		PCS* CX:M	Yes [ ] N/A [ ]
RM30	Register returns zero if the PCS does not implement the 10GBASE-X port type	45.2.3.9		PCS* !CX:M	Yes [ ] N/A [ ]
RM31	Writes to bit are ignored and reads return a value of zero	45.2.3.10.1		PCS* PX:M	Yes [ ] N/A [ ]
RM32	Setting the bits to <10> selects the mixed frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM33	Setting the bits to <01> selects the low-frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM34	Setting the bits to <00> selects the high-frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM35	Writes to 10GBASE-R PCS status 1 register have no effect	45.2.3.11		PCS* CR:M	Yes [ ] N/A [ ]
RM36	Reads from 10GBASE-R PCS status 1 register return zero for PCS that does not support 10GBASE-R	45.2.3.11		PCS* CR:M	Yes [ ] N/A [ ]
RM37	Writes to 10GBASE-R PCS status 2 register have no effect	45.2.3.12		PCS* CR:M	Yes [ ] N/A [ ]
RM38	Reads from 10GBASE-R PCS status 2 register return zero for PCS that does not support 10GBASE-R	45.2.3.12		PCS* CR:M	Yes [ ] N/A [ ]
RM39	Latched block lock implemented with latching low behavior	45.2.3.12.1		PCS* CR:M	Yes [ ] N/A [ ]
RM40	Latched high BER implemented with latching high behavior	45.2.3.12.2		PCS* CR:M	Yes [ ] N/A [ ]
RM41	BER counter clears to zero on read or reset	45.2.3.12.3		PCS* CR:M	Yes [ ] N/A [ ]
RM42	BER counter holds at all ones at overflow	45.2.3.12.3		PCS* CR:M	Yes [ ] N/A [ ]
RM43	Errored blocks counter implemented as a non roll over counter	45.2.3.12.4		PCS* CR:M	Yes [ ] N/A [ ]
RM44	Errored blocks counter clears to zero on read	45.2.3.12.4		PCS* CR:M	Yes [ ] N/A [ ]
RM45	Setting bit 3.42.5 to a one enables PRBS31 receive pattern testing if bit 3.32.2 is a one and bit 3.42.2 is not a one	45.2.3.15.1		PCS* PPT:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM46	Setting bit 3.42.5 to a zero disables PRBS31 receive pattern testing	45.2.3.15.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM47	Setting bit 3.42.4 to a one enables PRBS31 transmit pattern testing if bit 3.32.2 is a one and bit 3.42.3 is not a one	45.2.3.15.2		PCS* PPT:M	Yes [ ] N/A [ ]
RM48	Setting bit 3.42.4 to a zero disables PRBS31 transmit pattern testing	45.2.3.15.2		PCS* PPT:M	Yes [ ] N/A [ ]
RM49	Test-pattern error counter clears to zero on read or reset	45.2.3.16		PCS* CR:M	Yes [ ] N/A [ ]
RM50	Test-pattern error counter holds at all ones at overflow	45.2.3.16		PCS* CR:M	Yes [ ] N/A [ ]
RM51	Bit indicates fault when any PCS register indicates fault	45.2.3.2.1	If subtype is supported	PCS*EPC:O	Yes [ ] No [ ] N/A [ ]
RM53	Writing this bit to a one activates the PAF when link is established	45.2.3.18.3		PCS*PAF:M	Yes [ ] N/A [ ]
RM54	Writes to bit are ignored while link is active or initializing or if PAF is not supported	45.2.3.18.3		PCS*PAF:M	Yes [ ] N/A [ ]
RM55	Bits indicate device capabilities upon reset	45.2.3.19		PCS*PAF:M	Yes [ ] N/A [ ]
RM56	Writes to the register through any PCS MMD in the same package effect the register equally	45.2.3.19		PCS*PAF:M	Yes [ ] N/A [ ]
RM57	Single bit set to one and all others cleared to zero when device does not support aggregation of multiple PMEs	45.2.3.19		PCS:M	Yes [ ] N/A [ ]
RM58	PME aggregation used if one or more bits set	45.2.3.20		PCS*PAF:M	Yes [ ] N/A [ ]
RM59	Registers set to all zeros upon reset	45.2.3.20		PCS*PAF:M	Yes [ ] N/A [ ]
RM60	Writes to the register through any PCS MMD in the same package effect the register equally	45.2.3.20		PCS*PAF:M	Yes [ ] N/A [ ]
RM61	Bits reset to zero when read or upon MMD reset	45.2.3.21		PCS*PAF:M	Yes [ ] N/A [ ]
RM62	Bits held to one upon overflow	45.2.3.21		PCS*PAF:M	Yes [ ] N/A [ ]
RM63	Bits reset to zero when read or upon MMD reset	45.2.3.22		PCS*PAF:M	Yes [ ] N/A [ ]
RM64	Bits held to one upon overflow	45.2.3.22		PCS*PAF:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM65	Bits reset to zero when read or upon MMD reset	45.2.3.23		PCS*PAF:M	Yes [ ] N/A [ ]
RM66	Bits held to one upon overflow	45.2.3.23		PCS*PAF:M	Yes [ ] N/A [ ]
RM67	Bits reset to zero when read or upon MMD reset	45.2.3.24		PCS*PAF:M	Yes [ ] N/A [ ]
RM68	Bits held to one upon overflow	45.2.3.24		PCS*PAF:M	Yes [ ] N/A [ ]
RM69	Bits reset to zero when read or upon MMD reset	45.2.3.25		PCS*PAF:M	Yes [ ] N/A [ ]
RM70	Bits held to one upon overflow	45.2.3.25		PCS*PAF:M	Yes [ ] N/A [ ]
RM71	Bits reset to zero when read or upon MMD reset	45.2.3.26		PCS*PAF:M	Yes [ ] N/A [ ]
RM72	Bits held to one upon overflow	45.2.3.26		PCS*PAF:M	Yes [ ] N/A [ ]
RM73	Bits reset to zero when read or upon MMD reset	45.2.3.27		PCS*PAF:M	Yes [ ] N/A [ ]
RM74	Bits held to one upon overflow	45.2.3.27		PCS*PAF:M	Yes [ ] N/A [ ]
RM75	Bits reset to zero when read or upon MMD reset	45.2.3.28		PCS*PAF:M	Yes [ ] N/A [ ]
RM76	Bits held to one upon overflow	45.2.3.28		PCS*PAF:M	Yes [ ] N/A [ ]

45.5.3.8 PHY XS options

Item	Feature	Subclause	Value/Comment	Status	Support
*PL	Implementation of loopback	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]
*PT	Implementation of pattern testing	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]

45.5.3.9 PHY XS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	Device responds to all register addresses for that device	45.2		PX:M	Yes [ ] N/A [ ]
PM2	Writes to undefined and read-only registers have no effect	45.2		PX:M	Yes [ ] N/A [ ]
PM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PX:M	Yes [ ] N/A [ ]
PM4	Reserved and unsupported bits return a value of zero	45.2		PX:M	Yes [ ] N/A [ ]
PM5	Latching low bits remain low until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]
PM7	Latching high bits remain high until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]
PM9	Action on reset	45.2.4.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PX:M	Yes [ ] N/A [ ]
PM10	Return 1 until reset completed	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM11	Reset completes within 0.5 s	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM12	Device responds to reads of bits 4.0.15 and 4.8.15:14 during reset	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM13	Loopback mode	45.2.4.1.2	Whenever bit 4.0.14 is set to a one	PX*PL:M	Yes [ ] N/A [ ]
PM14	Receive data is returned on transmit path during loopback	45.2.4.1.2		PX*PL:M	Yes [ ] N/A [ ]
PM15	Writes to loopback bit are ignored and reads return zero	45.2.4.1.2		PX*!PL:M	Yes [ ] N/A [ ]
PM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.4.1.3		PX:M	Yes [ ] N/A [ ]
PM17	Speed selection bits 13 and 6 are written as one	45.2.4.1.4		PX:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PM18	Invalid writes to speed selection bits are ignored	45.2.4.1.4		PX:M	Yes [ ] N/A [ ]
PM19	Writes to status 1 register have no effect	45.2.4.2		PX:M	Yes [ ] N/A [ ]
PM20	Transmit link status implemented using latching low behavior	45.2.4.2.2		PX:M	Yes [ ] N/A [ ]
PM21	Unique identifier is composed of OUI, model number and revision	45.2.4.3		PX:M	Yes [ ] N/A [ ]
PM22	Writes to status 2 register have no effect	45.2.4.6		PX:M	Yes [ ] N/A [ ]
PM23	Transmit fault implemented with latching high behavior	45.2.4.6.2		PX:M	Yes [ ] N/A [ ]
PM24	Receive fault implemented with latching high behavior	45.2.4.6.3		PX:M	Yes [ ] N/A [ ]
PM25	Unique identifier is composed of OUI, model number and revision	45.2.4.7		PX:M	Yes [ ] N/A [ ]
PM26	Writes to 10G PHY XGXS Lane status register have no effect	45.2.4.8		PX:M	Yes [ ] N/A [ ]
PM27	Writes to bit are ignored and reads return a value of zero	45.2.4.9.1		PX*!PT:M	Yes [ ] N/A [ ]
PM28	Setting the bits to <10> selects the mixed frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]
PM29	Setting the bits to <01> selects the low-frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]
PM30	Setting the bits to <00> selects the high-frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]

45.5.3.10 DTE XS options

Item	Feature	Subclause	Value/Comment	Status	Support
*DT	Implementation of pattern testing	45.2.5		DX:O	Yes [ ] No [ ] N/A [ ]

45.5.3.11 DTE XS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
DM1	Device responds to all register addresses for that device	45.2		DX:M	Yes [ ] N/A [ ]
DM2	Writes to undefined and read-only registers have no effect	45.2		DX:M	Yes [ ] N/A [ ]
DM3	Operation is not affected by writes to reserved and unsupported bits	45.2		DX:M	Yes [ ] N/A [ ]
DM4	Reserved and unsupported bits return a value of zero	45.2		DX:M	Yes [ ] N/A [ ]
DM5	Latching low bits remain low until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM7	Latching high bits remain high until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM9	Action on reset	45.2.5.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	DX:M	Yes [ ] N/A [ ]
DM10	Return 1 until reset completed	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM11	Reset completes within 0.5 s	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM12	Device responds to reads of bits 5.0.15 and 5.8.15:14 during reset	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM13	Loopback mode	45.2.5.1.2	Whenever bit 5.0.14 is set to a one	DX:M	Yes [ ] N/A [ ]
DM14	Transmit data is returned on receive path during loopback	45.2.5.1.2		DX:M	Yes [ ] N/A [ ]
DM15	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.5.1.3		DX:M	Yes [ ] N/A [ ]
DM16	Speed selection bits 13 and 6 are written as one	45.2.5.1.4		DX:M	Yes [ ] N/A [ ]
DM17	Invalid writes to speed selection bits are ignored	45.2.5.1.4		DX:M	Yes [ ] N/A [ ]
DM18	Writes to status 1 register have no effect	45.2.5.2		DX:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
DM19	Receive link status implemented using latching low behavior	45.2.5.2.2		DX:M	Yes [ ] N/A [ ]
DM20	Unique identifier is composed of OUI, model number and revision	45.2.5.3		DX:M	Yes [ ] N/A [ ]
DM21	Writes to status 2 register have no effect	45.2.5.6		DX:M	Yes [ ] N/A [ ]
DM22	Transmit fault implemented with latching high behavior	45.2.5.6.2		DX:M	Yes [ ] N/A [ ]
DM23	Receive fault implemented with latching high behavior	45.2.5.6.3		DX:M	Yes [ ] N/A [ ]
DM24	Unique identifier is composed of OUI, model number and revision	45.2.5.7		DX:M	Yes [ ] N/A [ ]
DM25	Writes to 10G DTE XGXS Lane status register have no effect	45.2.5.8		DX:M	Yes [ ] N/A [ ]
DM26	Writes to bit are ignored and reads return a value of zero	45.2.5.9.1		DX*!DT:M	Yes [ ] N/A [ ]
DM27	Setting the bits to <10> selects the mixed frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]
DM28	Setting the bits to <01> selects the low-frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]
DM29	Setting the bits to <00> selects the high-frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]

45.5.3.12 Vendor specific MMD 1 management functions

Item	Feature	Subclause	Value/Comment	Status	Support
VSA1	Device responds to all register addresses for that device	45.2		VSA:M	Yes [ ] N/A [ ]
VSA2	Writes to undefined and read-only registers have no effect	45.2		VSA:M	Yes [ ] N/A [ ]
VSA3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSA:M	Yes [ ] N/A [ ]
VSA4	Reserved and unsupported bits return a value of zero	45.2		VSA:M	Yes [ ] N/A [ ]
VSA5	Unique identifier is composed of OUI, model number and revision	45.2.8.1		VSA:M	Yes [ ] N/A [ ]
VSA6	Writes to status register have no effect	45.2.8.2		VSA:M	Yes [ ] N/A [ ]
VSA7	Unique identifier is composed of OUI, model number and revision	45.2.8.3		VSA:M	Yes [ ] N/A [ ]

45.5.3.13 Vendor specific MMD 2 management functions

Item	Feature	Subclause	Value/Comment	Status	Support
VSB1	Device responds to all register addresses for that device	45.2		VSB:M	Yes [ ] N/A [ ]
VSB2	Writes to undefined and read-only registers have no effect	45.2		VSB:M	Yes [ ] N/A [ ]
VSB3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSB:M	Yes [ ] N/A [ ]
VSB4	Reserved and unsupported bits return a value of zero	45.2		VSB:M	Yes [ ] N/A [ ]
VSB5	Unique identifier is composed of OUI, model number and revision	45.2.9.1		VSB:M	Yes [ ] N/A [ ]
VSB6	Writes to status register have no effect	45.2.9.2		VSB:M	Yes [ ] N/A [ ]
VSB7	Unique identifier is composed of OUI, model number and revision	45.2.9.3		VSB:M	Yes [ ] N/A [ ]

45.5.3.14 Management frame structure

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Device has implemented sixteen bit address register	45.3		M	Yes [ ]
MF2	Address register is overwritten by address frames	45.3		M	Yes [ ]
MF3	Write, read, and post-read-increment-address frames access the register whose address is held in the address register	45.3		M	Yes [ ]
MF4	Write and read frames do not modify the address register	45.3		M	Yes [ ]
MF5	Post-read-increment-address frames increment the address register by one unless the address register contains 65 535	45.3		M	Yes [ ]
MF6	Components containing several MMDs implement separate address registers	45.3		M	Yes [ ]
MF7	Tri state drivers are disabled during idle	45.3.1		M	Yes [ ]
MF8	STA sources 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF9	MMD observes 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF10	Frames containing ST=<01> sequence are ignored	45.3.3		M	Yes [ ]
MF11	STA tri state driver is high impedence during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF12	MMD tri state driver is high impedence during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF13	MMD tri state driver drives a zero bit during second bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF14	STA tri state driver drives a one bit followed by a zero bit for the TA during write or address frames	45.3.7		M	Yes [ ]
MF15	First bit transmitted and received is bit 15	45.3.8		M	Yes [ ]

45.5.3.15 TC management functions

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Device responds to all register addresses for that device	45.2		TC:M	Yes [ ] N/A [ ]
TC2	Writes to undefined and read only register have no effect	45.2		TC:M	Yes [ ] N/A [ ]
TC3	Operation is not affected by writes to reserved and unsupported bits	45.2		TC:M	Yes [ ] N/A [ ]
TC4	Reserved and unsupported bits return a value of zero	45.2		TC:M	Yes [ ] N/A [ ]
TC5	Setting bit to a one sets all TC registers to their default states	45.2.6.1.1		TC:M	Yes [ ] N/A [ ]
TC6	Bit reads one while reset is in progress otherwise reads zero	45.2.6.1.1		TC:M	Yes [ ] N/A [ ]
TC7	Control and management interface is restored within 0.5s from setting bit to a one	45.2.6.1.1		TC:M	Yes [ ] N/A [ ]
TC8	During reset, TC responds to reads from bit	45.2.6.1.1		TC:M	Yes [ ] N/A [ ]
TC9	Writes that would select an unsupported speed are ignored	45.2.6.1.2		TC:M	Yes [ ] N/A [ ]
TC10	Identifier composed properly	45.2.6.2		TC:M	Yes [ ] N/A [ ]
TC11	Identifier composed properly	45.2.6.5		TC:M	Yes [ ] N/A [ ]
TC12	Register is unique across all PCS MMDs in a package	45.2.6.6		TC:M	Yes [ ] N/A [ ]
TC13	Operation ignored when link is up or initializing	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC14	Bits indicate “Ready” when PAF is capable	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC15	Writes ignored and “Ready” indicated if PAF is unsupported	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC16	Bits indicate “Ready” when operation is complete or upon reset	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC17	Bits read as zero if PAF is unsupported	45.2.6.7.1		TC:M	Yes [ ] N/A [ ]
TC18	Bits read as zero if PAF is unsupported	45.2.6.7.2		TC:M	Yes [ ] N/A [ ]
TC19	Register is unique across all PCS MMDs in a package	45.2.6.8		TC:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TC20	Register is unique across all PCS MMDs in a package	45.2.6.9		TC:M	Yes [ ] N/A [ ]
TC21	Operation ignored when link is up or initializing	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC22	Bits indicate “Ready” when PAF is capable	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC23	Writes ignored and “Ready” indicated if PAF is unsupported	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC24	Bits indicate “Ready” when operation is complete or on reset	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC25	Register is unique across all PCS MMDs in a package	45.2.6.10		TC:M	Yes [ ] N/A [ ]
TC26	Bits reset to zero when read or reset	45.2.6.11		TC:M	Yes [ ] N/A [ ]
TC27	Bits held to one upon overflow	45.2.6.11		TC:M	Yes [ ] N/A [ ]
TC28	Bits reset to zero when read or reset	45.2.6.12		TC:M	Yes [ ] N/A [ ]
TC29	Bits held to one upon overflow	45.2.6.12		TC:M	Yes [ ] N/A [ ]

45.5.3.16 Clause 22 extension options

Item	Feature	Subclause	Value/Comment	Status	Support
*FEC	Implementation of PHY FEC	65.4.4.6		CTT:O	Yes [ ] No [ ] N/A [ ]

45.5.3.17 Clause 22 extension management functions

Item	Feature	Subclause	Value/Comment	Status	Support
CT1	Device responds to all register addresses for that device	45.2		CTT:M	Yes [ ] N/A [ ]
CT2	Writes to undefined and read only register have no effect	45.2		CTT:M	Yes [ ] N/A [ ]
CT3	Operation is not affected by writes to reserved and unsupported bits	45.2		CTT:M	Yes [ ] N/A [ ]
CT4	Reserved and unsupported bits return a value of zero	45.2		CTT:M	Yes [ ] N/A [ ]
CT5	Bits set to zero upon PHY reset	45.2.7.3.1		CTT*FEC:M	Yes [ ] N/A [ ]
CT6	Bits reset to all zeros when the register is read by the management function or upon PHY reset.	45.2.7.4		CTT*FEC:M	Yes [ ] N/A [ ]
CT7	Bits held at all ones in the case of overflow	45.2.7.4		CTT*FEC:M	Yes [ ] N/A [ ]
CT8	Bits reset to all zeros when the register is read by the management function or upon PHY reset.	45.2.7.5		CTT*FEC:M	Yes [ ] N/A [ ]
CT9	Bits held at all ones in the case of overflow	45.2.7.5		CTT*FEC:M	Yes [ ] N/A [ ]
CT10	Bits reset to all zeros when the register is read by the management function or upon PHY reset.	45.2.7.6		CTT*FEC:M	Yes [ ] N/A [ ]
CT11	Bits held at all ones in the case of overflow	45.2.7.6		CTT*FEC:M	Yes [ ] N/A [ ]

45.5.3.18 Signal timing characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
ST1	MDIO setup and hold time	45.4.2	Setup min = 10 ns; Hold min = 10 ns per	M	Yes [ ]
ST2	MDIO clock to output delay	45.4.2	Min = 0 ns; Max = 300 ns per	M	Yes [ ]
ST3	MDC min high/low time	45.4.2	160 ns	M	Yes [ ]
ST4	MDC min period	45.4.2	400 ns	M	Yes [ ]

45.5.3.19 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	V_{OH}	45.4.1	≥ 1.0 V (I_{OH} = –100 uA) ≤ 1.5 V (I_{OH} = –100 uA)	M	Yes [ ]
EC2	V_{OL}	45.4.1	≥ –0.3 V (I_{OL} = 100 uA) ≤ 0.2 V (I_{OL} = 100 uA)	M	Yes [ ]
EC3	V_{IH}	45.4.1	0.84 V ≤ V_{IH} ≤ 1.5 V	M	Yes [ ]
EC4	V_{IL}	45.4.1	–0.3 ≤ V_{IL} ≤ 0.36 V	M	Yes [ ]
EC5	Input capacitance for MDIO	45.4.1	≤ 10 pF	M	Yes [ ]
EC6	Total capacitive load	45.4.1	≤ 470 pF	M	Yes [ ]
EC7	I_{OH}	45.4.1	≤ –4 mA at V_{OH} = 1.0 V	!ODB:M	Yes [ ] N/A[ ]
EC8	I_{OL}	45.4.1	≥ +4 mA at V_{OL} = 0.2 V	M	Yes [ ]