22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.1 Overview

This clause defines the logical, electrical, and mechanical characteristics for the Reconciliation Sublayer (RS) and Media Independent Interface (MII) between CSMA/CD media access controllers and various PHYs. Figure 22–1 shows the relationship of the Reconciliation sublayer and MII to the ISO/IEC OSI reference model.

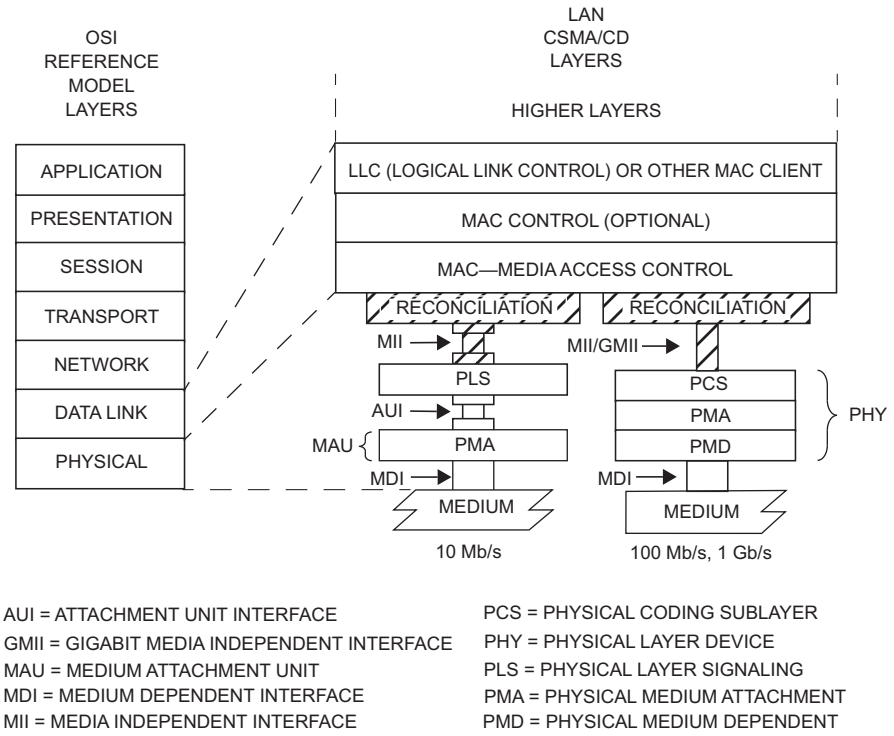

Figure 22–1—MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayers and PHYs for data transfer at 10 Mb/s and 100 Mb/s, and between Station Management (STA) and PHY entities supporting data transfer at 10 Mb/s or above (see 22.2.4).

This interface has the following characteristics:

a) It is capable of supporting 10 Mb/s and 100 Mb/s rates for data transfer, and management functions for PHYs supporting data transfer at 10 Mb/s or above (see 22.2.4).
b) Data and delimiters are synchronous to clock references.
c) It provides independent four bit wide transmit and receive data paths.
d) It uses TTL signal levels, compatible with common digital CMOS ASIC processes.
e) It provides a simple management interface.
f) It is capable of driving a limited length of shielded cable.
g) It provides full duplex operation.

22.1.1 Summary of major concepts

a) Each direction of data transfer is serviced with seven (making a total of 14) signals: Data (a four-bit bundle), Delimiter, Error, and Clock.
b) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.
c) A management interface comprised of two signals provides access to management parameters and services.
d) The Reconciliation sublayer maps the signal set provided at the MII to the PLS service definition specified in Clause 6.

22.1.2 Application

This clause applies to the interface between MAC sublayer and PHYs, and between PHYs and Station Management entities. The implementation of the interface may assume any of the following three forms:

a) A chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board.
b) A motherboard to daughterboard interface between two or more printed circuit boards.
c) An interface between two printed circuit assemblies that are attached with a length of cable and an appropriate connector.

Figure 22–2 provides an example of the third application environment listed above. All MII conformance tests are performed at the mating surfaces of the MII connector, identified by the line A-A.

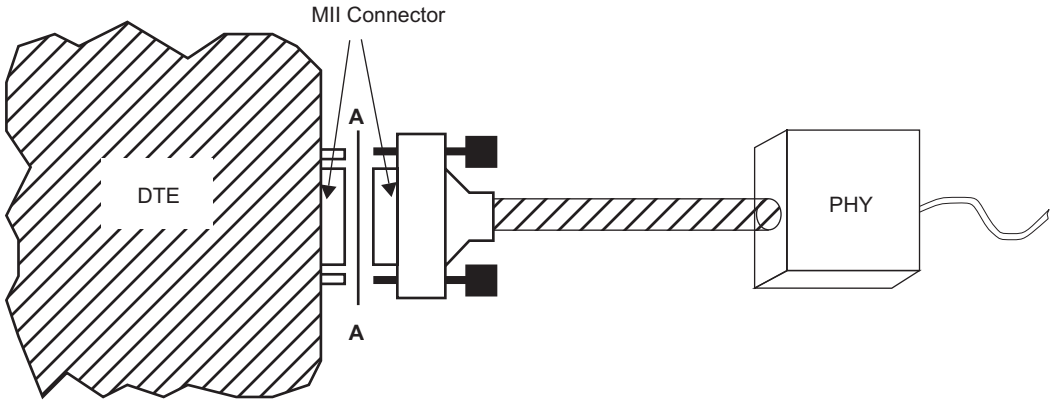

Figure 22–2—Example application showing location of conformance test

This interface is used to provide media independence for various forms of unshielded twisted-pair wiring, shielded twisted-pair wiring, fiber optic cabling, and potentially other media, so that identical media access controllers may be used with any of these media.

To allow for the possibility that multiple PHYs may be controlled by a single station management entity, the MII management interface has provisions to accommodate up to 32 PHYs, with the restriction that a maximum of one PHY may be attached to a management interface via the mechanical interface defined in 22.6.

22.1.3 Rates of operation

The MII can support two specific data rates, 10 Mb/s and 100 Mb/s. The functionality is identical at both data rates, as are the signal timing relationships. The only difference between 10 Mb/s and 100 Mb/s operation is the nominal clock frequency.

PHYs that provide an MII are not required to support both data rates, and may support either one or both. PHYs must report the rates they are capable of operating at via the management interface, as described in 22.2.4.

22.1.4 Allocation of functions

The allocation of functions at the MII is such that it readily lends itself to implementation in both PHYs and MAC sublayer entities. The division of functions balances the need for media independence with the need for a simple and cost-effective interface.

While the Attachment Unit Interface (AUI) was defined to exist between the Physical Signaling (PLS) and Physical Media Attachment (PMA) sublayers for 10 Mb/s DTEs, the MII maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO (IEEE) seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling of the PLS or PCS sublayer and the PMA sublayer.

22.1.5 Relationship of MII and GMII

The Gigabit Media Independent Interface (GMII) is similar to the MII. The GMII uses the MII management interface and register set specified in 22.2.4. These common elements of operation allow Station Management to determine PHY capabilities for any supported speed of operation and configure the station based on those capabilities. In a station supporting both MII and GMII operation, configuration of the station would include enabling either the MII or GMII operation as appropriate for the data rate of the selected PHY.

Most of the MII and GMII signals use the same names, but the width of the RXD and TXD data bundles and the semantics of the associated control signals differ between MII and GMII operation. The GMII transmit path clocking also differs significantly from MII clocking. MII operation of these signals and clocks is specified within Clause 22 and GMII operation is specified within Clause 35.

22.2 Functional specifications

The MII is designed to make the differences among the various media absolutely transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end. Additionally, the MII is designed to be easily implemented at minimal cost using conventional design techniques and manufacturing processes.

22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The MII signals are defined in detail in 22.2.2.

Figure 22–3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the station management entity (STA).

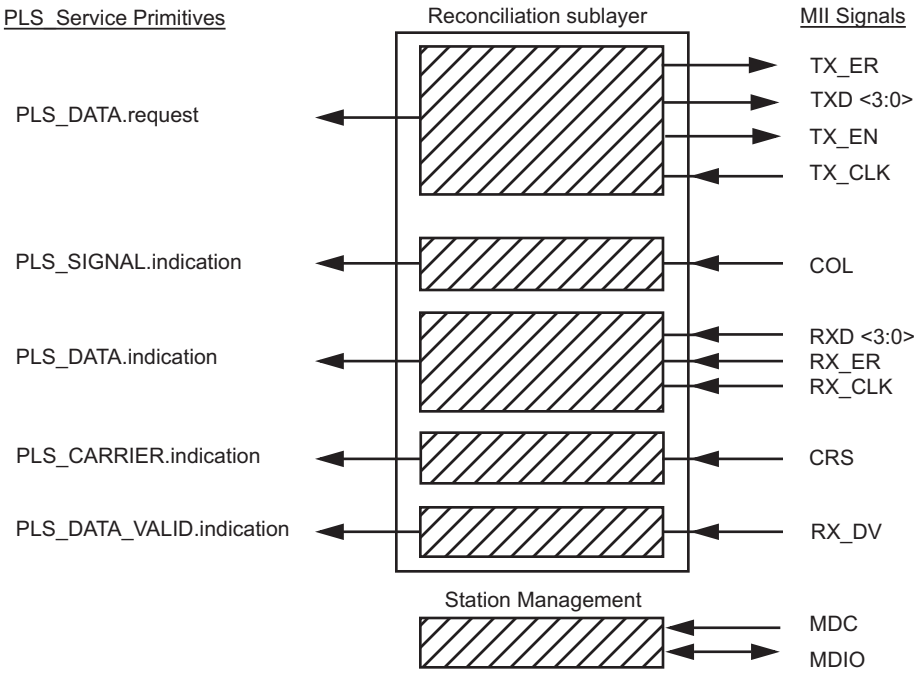

Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII

22.2.1.1 Mapping of PLS_DATA.request

22.2.1.1.1 Function

Map the primitive PLS_DATA.request to the MII signals TXD<3:0>, TX_EN and TX_CLK.

22.2.1.1.2 Semantics of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the signals TXD<3>, TXD<2>, TXD<1> and TXD<0>, each of which conveys one bit of data while TX_EN is asserted. The value DATA_COMPLETE is conveyed by the de-assertion of TX_EN. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the TX_CLK signal.

22.2.1.1.3 When generated

The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the Reconciliation sublayer after every group of four PLS_DATA.request transactions from the MAC sublayer to request the transmission of four data bits on the physical medium or to stop transmission.

22.2.1.2 Mapping of PLS_DATA.indication

22.2.1.2.1 Function

Map the primitive PLS_DATA.indication to the MII signals RXD<3:0>, RX_DV, RX_ER, and RX_CLK.

22.2.1.2.2 Semantics of the service primitive

PLS_DATA.indication (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: ONE or ZERO. It represents a single data bit. The values ONE and ZERO are derived from the signals RXD<3>, RXD<2>, RXD<1>, and RXD<0>, each of which represents one bit of data while RX_DV is asserted.

The value of the data transferred to the MAC is controlled by the RX_ER signal, see 22.2.1.5, Response to RX_ER indication from MII.

Synchronization between the PHY and the Reconciliation sublayer is achieved by way of the RX_CLK signal.

22.2.1.2.3 When generated

This primitive is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued. Each nibble of data transferred on RXD<3:0> will result in the generation of four PLS_DATA.indication transactions.

22.2.1.3 Mapping of PLS_CARRIER.indication

22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indication to the MII signal CRS.

22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF are derived from the MII signal CRS.

22.2.1.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

While the RX_DV signal is de-asserted, any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value. At any time after CRS and RX_DV are both asserted, de-assertion of RX_DV must cause CARRIER_STATUS to transition to the CARRIER_OFF value. This transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value must be recognized by the MAC sublayer, even if the CRS signal is still asserted at the time.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is

described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to the carrierSense variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC process BitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

22.2.1.4 Mapping of PLS_SIGNAL.indication

22.2.1.4.1 Function

Map the primitive PLS_SIGNAL.indication to the MII signal COL.

22.2.1.4.2 Semantics of the service primitive

PLS_SIGNAL.indication (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. SIGNAL_STATUS assumes the value SIGNAL_ERROR when the MII signal COL is asserted, and assumes the value NO_SIGNAL_ERROR when COL is de-asserted.

22.2.1.4.3 When generated

The PLS_SIGNAL.indication service primitive is generated whenever SIGNAL_STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

22.2.1.5 Response to RX_ER indication from MII

If, during frame reception, both RX_DV and RX_ER are asserted, the Reconciliation sublayer shall ensure that the MAC will detect a FrameCheckError in that frame.

This requirement may be met by incorporating a function in the Reconciliation sublayer that produces a result that is guaranteed to be not equal to the CRC result, as specified by the algorithm in 3.2.8, of the sequence of nibbles comprising the received frame as delivered to the MAC sublayer. The Reconciliation sublayer must then ensure that the result of this function is delivered to the MAC sublayer at the end of the received frame in place of the last nibble(s) received from the MII.

Other techniques may be employed to respond to RX_ER, provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

22.2.1.6 Conditions for generation of TX_ER

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then the signal TX_ER may be generated.

For example, a repeater that detects an RX_ER during frame reception on an input port may propagate that error indication to its output ports by asserting TX_ER during the process of transmitting that frame.

Since there is no mechanism in the definition of the MAC sublayer by which the transmit data stream can be deliberately corrupted, the Reconciliation sublayer is not required to generate TX_ER.

22.2.1.7 Mapping of PLS_DATA_VALID.indication

22.2.1.7.1 Function

Map the primitive PLS_DATA_VALID.indication to the MII signal RX_DV.

22.2.1.7.2 Semantics of the service primitive

PLS_DATA_VALID.indication (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. DATA_VALID_STATUS assumes the value DATA_VALID when the MII signal RX_DV is asserted, and assumes the value DATA_NOT_VALID when RX_DV is de-asserted.

22.2.1.7.3 When generated

The PLS_DATA_VALID.indication service primitive is generated by the Reconciliation sublayer whenever the DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

22.2.2 MII signal functional specifications

22.2.2.1 TX_CLK (transmit clock)

TX_CLK (Transmit Clock) is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals from the Reconciliation sublayer to the PHY. TX_CLK is sourced by the PHY.

The TX_CLK frequency shall be 25% of the nominal transmit data rate ± 100 ppm. For example, a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz, and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. The duty cycle of the TX_CLK signal shall be between 35% and 65% inclusive.

NOTE—See additional information in 22.2.4.1.5.

22.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals from the PHY to the Reconciliation sublayer. RX_CLK is sourced by the PHY. The PHY may recover the RX_CLK reference from the received data or it may derive the RX_CLK reference from a nominal clock (e.g., the TX_CLK reference).

The minimum high and low times of RX_CLK shall be 35% of the nominal period under all conditions.

While RX_DV is asserted, RX_CLK shall be synchronous with recovered data, shall have a frequency equal to 25% of the data rate of the received signal, and shall have a duty cycle of between 35% and 65% inclusive.

When the signal received from the medium is continuous and the PHY can recover the RX_CLK reference and supply the RX_CLK on a continuous basis, there is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference.

Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall be made only while RX_DV is de-asserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the de-assertion of RX_DV at the end of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period.

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5.

22.2.2.3 TX_EN (transmit enable)

TX_EN indicates that the Reconciliation sublayer is presenting nibbles on the MII for transmission. It shall be asserted by the Reconciliation sublayer synchronously with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the MII. TX_EN shall be negated prior to the first TX_CLK following the final nibble of a frame. TX_EN is driven by the Reconciliation sublayer and shall transition synchronously with respect to the TX_CLK.

Figure 22–4 depicts TX_EN behavior during a frame transmission with no collisions.

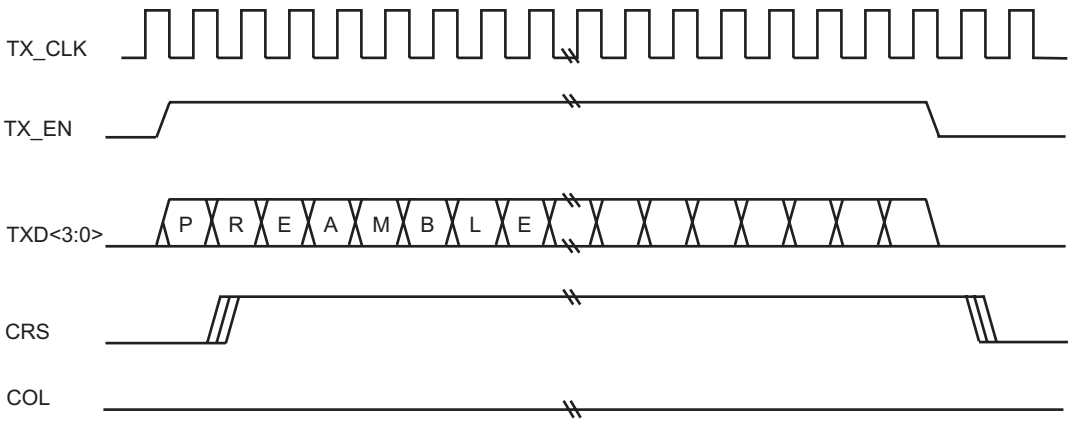

Figure 22–4—Transmission with no collision

22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0 >is the least significant bit. While TX_EN is de-asserted, TXD<3:0> shall have no effect upon the PHY.

Figure 22–4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

22.2.2.5 TX_ER (transmit coding error)

TX_ER shall transition synchronously with respect to the TX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PHY shall emit one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.

Assertion of the TX_ER signal shall not affect the transmission of data when a PHY is operating at 10 Mb/s, or when TX_EN is de-asserted.

Figure 22–5 shows the behavior of TX_ER during the transmission of a frame propagating an error.

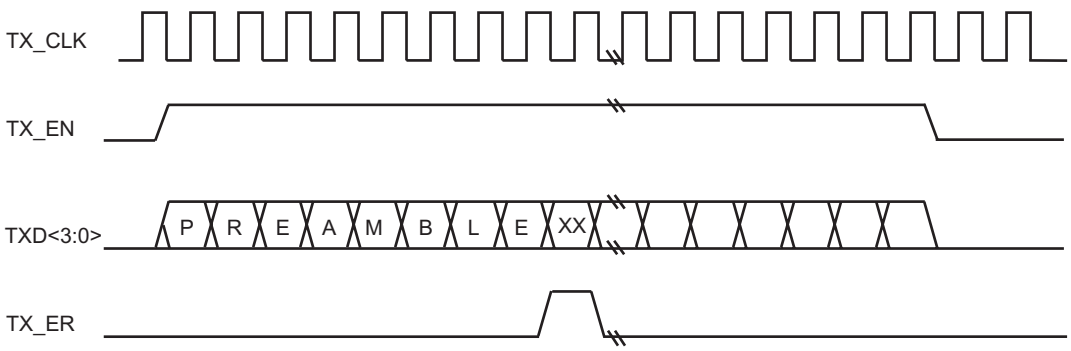

Figure 22–5—Propagating an error

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

The TX_ER signal shall be implemented at the MII of a PHY, may be implemented at the MII of a repeater that provides an MII port, and may be implemented in MAC sublayer devices. If a Reconciliation sublayer or a repeater with an MII port does not actively drive the TX_ER signal, it shall ensure that the TX_ER signal is pulled down to an inactive state at all times.

22.2.2.6 RX_DV (Receive Data Valid)

RX_DV (Receive Data Valid) is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on the RXD<3:0> bundle and that the data on RXD<3:0> is synchronous to RX_CLK. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall remain asserted continuously from the first recovered nibble of the frame through the final recovered nibble and shall be negated prior to the first RX_CLK that follows the final nibble. In order for a received frame to be correctly interpreted by the Reconciliation sublayer and the MAC sublayer, RX_DV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

Figure 22–6 shows the behavior of RX_DV during frame reception.

22.2.2.7 RXD (receive data)

RXD is a bundle of four data signals (RXD<3:0>) that transition synchronously with respect to the RX_CLK. RXD<3:0> are driven by the PHY. For each RX_CLK period in which RX_DV is asserted, RXD<3:0> transfer four bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the

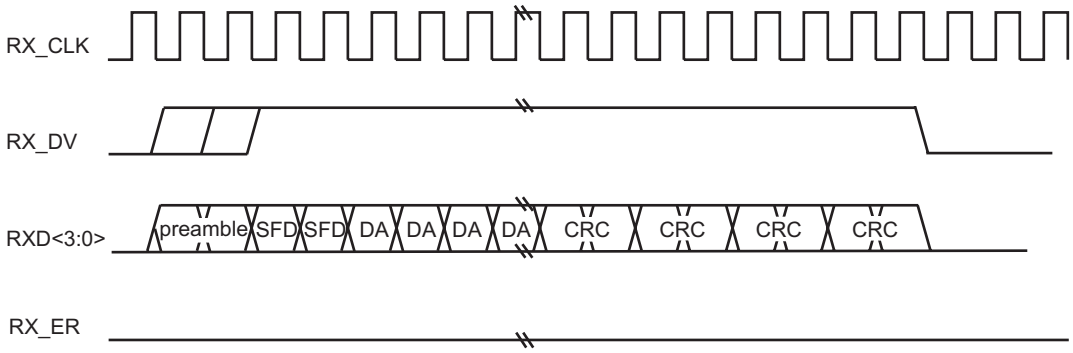

Figure 22–6—Reception with no errors

least significant bit. While RX_DV is de-asserted, RXD<3:0> shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the value <1110> onto RXD<3:0>. See 22.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the MII. In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<3:0> back to RXD<3:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <3:0> must not be looped back to RXD <3:0> unless the loopback mode of operation is selected.

Figure 22–6 shows the behavior of RXD<3:0> during frame reception.

Table 22–2 summarizes the permissible encoding of RXD<3:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

22.2.2.8 RX_ER (receive error)

RX_ER (Receive Error) is driven by the PHY. RX_ER shall be asserted for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer. RX_ER shall transition synchronously with respect to RX_CLK. While RX_DV is de-asserted, RX_ER shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal for at least one cycle of the RX_CLK while driving the appropriate value onto RXD<3:0>, as defined in 22.2.2.7. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

The effect of RX_ER on the Reconciliation sublayer is defined in 22.2.1.5, Response to RX_ER indication from MII.

Figure 22–7 shows the behavior of RX_ER during the reception of a frame with errors.

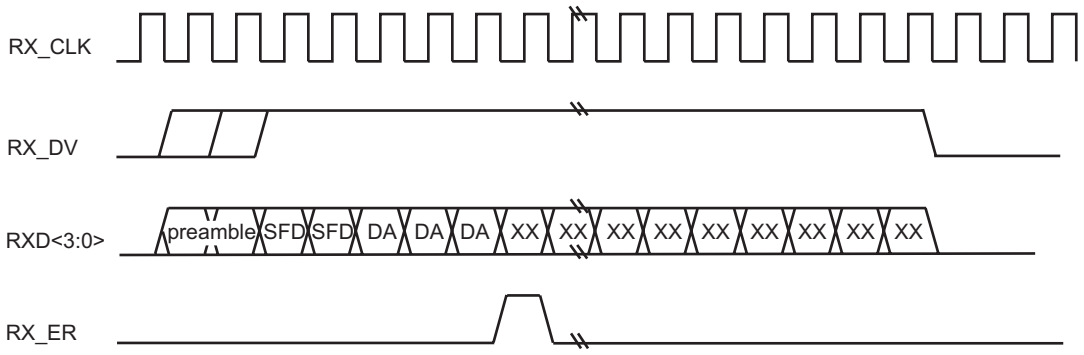

Figure 22–7—Reception with errors

Figure 22–8 shows the behavior of RX_ER, RX_DV and RXD<3:0> during a False Carrier indication.

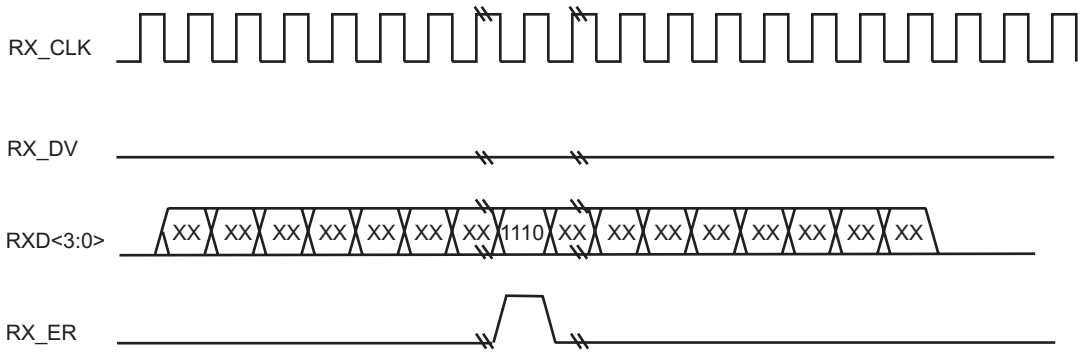

Figure 22–8—False Carrier indication

22.2.2.9 CRS (carrier sense)

CRS shall be asserted by the PHY when either the transmit or receive medium is nonidle. CRS shall be de-asserted by the PHY when both the transmit and receive media are idle. The PHY shall ensure that CRS remains asserted throughout the duration of a collision condition.

CRS is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the CRS signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22–4 shows the behavior of CRS during a frame transmission without a collision, while Figure 22–9 shows the behavior of CRS during a frame transmission with a collision.

22.2.2.10 COL (collision detected)

COL shall be asserted by the PHY upon detection of a collision on the medium, and shall remain asserted while the collision condition persists.

COL shall be asserted by a PHY that is operating at 10 Mb/s in response to a *signal_quality_error* message from the PMA.

COL is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the COL signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22–9 shows the behavior of COL during a frame transmission with a collision.

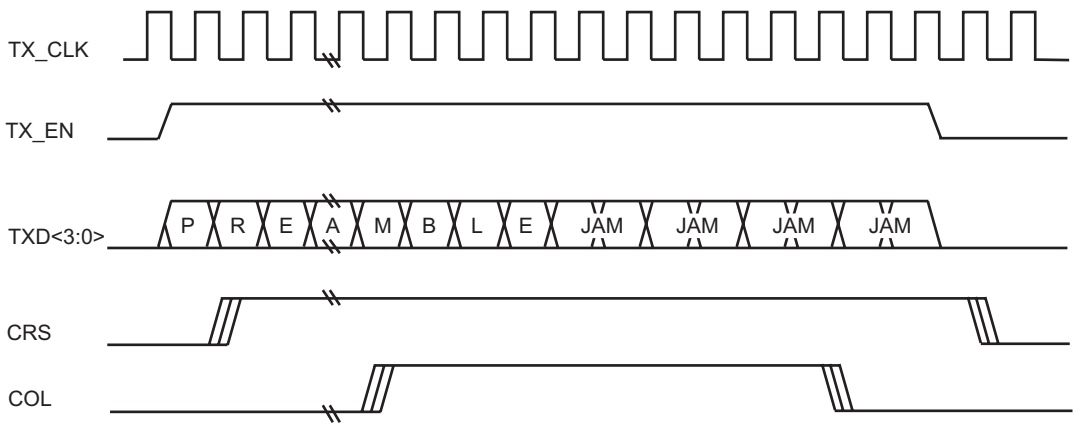

Figure 22–9—Transmission with collision

NOTE—The circuit assembly that contains the Reconciliation sublayer may incorporate a weak pull-up on the COL signal as a means of detecting an open circuit condition on the COL signal at the MII. The limit on the value of this pull-up is defined in 22.4.4.2.

22.2.2.11 MDC (management data clock)

MDC is sourced by the station management entity to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MDC shall be 160 ns each, and the minimum period for MDC shall be 400 ns, regardless of the nominal period of TX_CLK and RX_CLK.

22.2.2.12 MDIO (management data input/output)

MDIO is a bidirectional signal between the PHY and the STA. It is used to transfer control information and status between the PHY and the STA. Control information is driven by the STA synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the STA.

MDIO shall be driven through three-state circuits that enable either the STA or the PHY to drive the signal. A PHY that is attached to the MII via the mechanical interface specified in 22.6 shall provide a resistive pull-up to maintain the signal in a high state. The STA shall incorporate a resistive pull-down on the MDIO signal and thus may use the quiescent state of MDIO to determine if a PHY is connected to the MII via the mechanical interface defined in 22.6. The limits on the values of these pull-ups and pull-downs are defined in 22.4.4.2.

22.2.3 Frame structure

Data frames transmitted through the MII shall have the frame format shown in Figure 22–10.

<inter-frame><preamble><sfd><data><efd>

Figure 22–10—MII frame format

For the MII, transmission and reception of each octet of data shall be done a nibble at a time with the order of nibble transmission and reception as shown in Figure 22–11.

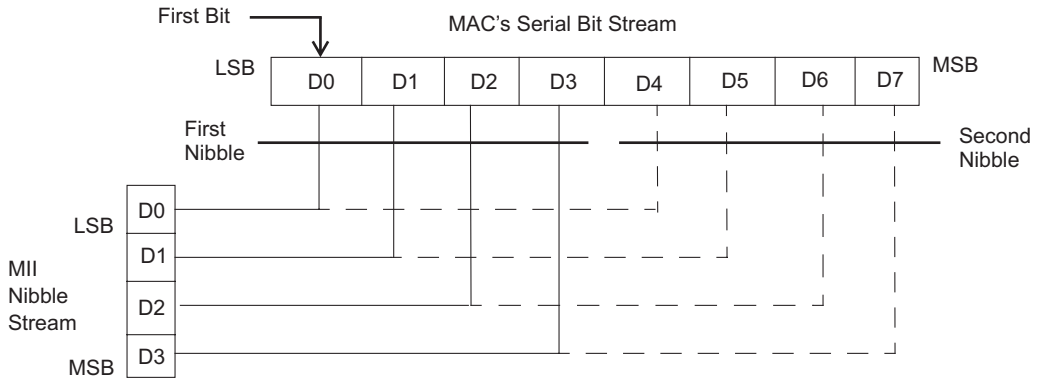

Figure 22–11—Octet/nibble transmit and receive order

The bits of each octet are transmitted and received as two nibbles, bits 0 through 3 of the octet corresponding to bits 0 through 3 of the first nibble transmitted or received, and bits 4 through 7 of the octet corresponding to bits 0 through 3 of the second nibble transmitted or received.

22.2.3.1 Inter-frame

The inter-frame period provides an observation window for an unspecified amount of time during which no data activity occurs on the MII. The absence of data activity is indicated by the de-assertion of the RX_DV signal on the receive path, and the de-assertion of the TX_EN signal on the transmit path. The MAC inter-FrameSpacing parameter defined in Clause 4 is measured from the de-assertion of the CRS signal to the assertion of the CRS signal.

22.2.3.2 Preamble and start of frame delimiter

22.2.3.2.1 Transmit case

The preamble <preamble> begins a frame transmission. The bit value of the preamble field at the MII is unchanged from that specified in 7.2.3.2 and shall consist of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

In the preceding example, the preamble is displayed using the bit order it would have if transmitted serially. This means that for each octet the leftmost l value represents the LSB of the octet, and the rightmost 0 value the octet MSB.

The SFD (Start Frame Delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value of the SFD at the MII is unchanged from that specified in 7.2.3.3 and is the bit sequence:

10101011

The preamble and SFD shall be transmitted through the MII as nibbles starting from the assertion of TX_EN as shown in Table 22–3.

Table 22–3—Transmitted preamble and SFD

Signal	Bit values of nibbles transmitted through MII																		
TXD0	X	1[a]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[b]	1	D0[c]	D4[d]
TXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[a]1st preamble nibble transmitted.
[b]1st SFD nibble transmitted.
[c]1st data nibble transmitted.
[d]D0 through D7 are the first eight bits of the data field from the Protocol Data Unit (PDU).

22.2.3.2.2 Receive case

The conditions for assertion of RX_DV are defined in 22.2.2.6.

The alignment of the received SFD and data at the MII shall be as shown in Table 22–4 and Table 22–5. Table 22–4 depicts the case where no preamble nibbles are conveyed across the MII, and Table 22–5 depicts the case where the entire preamble is conveyed across the MII.

Table 22–4—Start of receive with no preamble preceding SFD

Signal	Bit values of nibbles received through MII										
RXD0	X	X	X	X	X	X	X	1[a]	1	D0[b]	D4[c]
RXD1	X	X	X	X	X	X	X	0	0	D1	D5
RXD2	X	X	X	X	X	X	X	1	1	D2	D6
RXD3	X	X	X	X	X	X	X	0	1	D3	D7
RX_DV	0	0	0	0	0	0	0	1	1	1	1

[a]1st SFD nibble received.
[b]1st data nibble received.
[c]D0 through D7 are the first eight bits of the data field from the PDU.

Table 22–5—Start of receive with entire preamble preceding SFD

Signal	Bit values of nibbles received through MII																		
RXD0	X	1[a]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[b]	1	D0[c]	D4[d]
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[a]1st preamble nibble received.
[b]1st SFD nibble received.
[c]1st data nibble received.
[d]D0 through D7 are the first eight bits of the data field from the PDU.

22.2.3.3 Data

The data in a well formed frame shall consist of N octets of data transmitted as 2N nibbles. For each octet of data the transmit order of each nibble is as specified in Figure 22–11. Data in a collision fragment may consist of an odd number of nibbles.

22.2.3.4 End-of-Frame delimiter (EFD)

De-assertion of the TX_EN signal constitutes an End-of-Frame delimiter for data conveyed on TXD<3:0>, and de-assertion of RX_DV constitutes an End-of-Frame delimiter for data conveyed on RXD<3:0>.

22.2.3.5 Handling of excess nibbles

An excess nibble condition occurs when an odd number of nibbles is conveyed across the MII beginning with the SFD and including all nibbles conveyed until the End-of-Frame delimiter. Reception of a frame containing a non-integer number of octets shall be indicated by the PHY as an excess nibble condition.

Transmission of an excess nibble may be handled by the PHY in an implementation-specific manner. No assumption should be made with regard to truncation, octet padding, or exact nibble transmission by the PHY.

22.2.4 Management functions

The management interface specified here provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface.

The management interface consists of a pair of signals that physically transport the management information across the MII or GMII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. The register definition specifies a basic register set with an extension mechanism. The MII uses two basic registers. The GMII also uses the same two basic registers and adds a third basic register.

The MII basic register set consists of two registers referred to as the Control register (Register 0) and the Status register (Register 1). All PHYs that provide an MII shall incorporate the basic register set. All PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15). The status and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through 14 are part of the extended register set. The format of Registers 4 through 10 are defined for the specific Auto-Negotiation protocol used (Clause 28 or Clause 37). The format of these registers is selected by the bit settings of Registers 1 and 15.

The full set of management registers is listed in Table 22–6.

Table 22–6—MII management register set

Register address	Register name	Basic/Extended	
		MII	GMII
0	Control	B	B
1	Status	B	B
2,3	PHY Identifier	E	E
4	Auto-Negotiation Advertisement	E	E
5	Auto-Negotiation Link Partner Base Page Ability	E	E
6	Auto-Negotiation Expansion	E	E
7	Auto-Negotiation Next Page Transmit	E	E
8	Auto-Negotiation Link Partner Received Next Page	E	E
9	MASTER-SLAVE Control Register	E	E
10	MASTER-SLAVE Status Register	E	E
11	PSE Control register	E	E
12	PSE Status register	E	E
13	MMD Access Control Register	E	E
14	MMD Access Address Data Register	E	E
15	Extended Status	Reserved	B
16 through 31	Vendor Specific	E	E

22.2.4.1 Control register (Register 0)

The assignment of bits in the Control Register is shown in Table 22–7 below. The default value for each bit of the Control Register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 22–7—Control register bit definitions

Bit(s)	Name	Description	R/W[a]
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W
0.13	Speed Selection (LSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.12	Auto-Negotiation Enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
0.11	Power Down	1 = power down 0 = normal operation[b]	R/W
0.10	Isolate	1 = electrically Isolate PHY from MII or GMII 0 = normal operation[b]	R/W
0.9	Restart Auto-Negotiation	1 = restart Auto-Negotiation process 0 = normal operation	R/W SC
0.8	Duplex Mode	1 = full duplex 0 = half duplex	R/W
0.7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	R/W
0.6	Speed Selection (MSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.5	Unidirectional enable	When bit 0.12 is one or bit 0.8 is zero, this bit is ignored. When bit 0.12 is zero and bit 0.8 is one: 1 = Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = Enable transmit from media independent interface only when the PHY has determined that a valid link has been established	R/W
0.4:0	Reserved	Write as 0, ignore on read	R/W

[a]R/W = Read/Write, SC = Self-Clearing.
[b]For normal operation, both 0.10 and 0.11 must be cleared to zero; see 22.2.4.1.5.

22.2.4.1.1 Reset

Resetting a PHY is accomplished by setting bit 0.15 to a logic one. This action shall set the status and control registers to their default states. As a consequence this action may change the internal state of the PHY and the state of the physical link associated with the PHY. This bit is self-clearing, and a PHY shall return a value of one in bit 0.15 until the reset process is completed. A PHY is not required to accept a write transaction to the control register until the reset process is completed, and writes to bits of the control register other than 0.15 may have no effect until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 0.15.

The default value of bit 0.15 is zero.

NOTE—This operation may interrupt data communication.

22.2.4.1.2 Loopback

The PHY shall be placed in a loopback mode of operation when bit 0.14 is set to a logic one. When bit 0.14 is set, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII or GMII shall not result in the transmission of data on the network medium. When bit 0.14 is set, the PHY shall accept data from the MII or GMII transmit data path and return it to the MII or GMII receive data path in response to the assertion of TX_EN. When bit 0.14 is set, the delay from the assertion of TX_EN to the assertion of RX_DV shall be less than 512 BT. When bit 0.14 is set, the COL signal shall remain deasserted at all times, unless bit 0.7 is set, in which case the COL signal shall behave as described in 22.2.4.1.9. Clearing bit 0.14 to zero allows normal operation.

The default value of bit 0.14 is zero.

NOTE—The signal path through the PHY that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths through a PHY may be enabled via the extended register set, in an implementation-specific fashion.

22.2.4.1.3 Speed selection

Link speed can be selected via either the Auto-Negotiation process, or manual speed selection. Manual speed selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled and bit 0.6 is cleared to a logic zero, setting bit 0.13 to a logic one configures the PHY for 100 Mb/s operation, and clearing bit 0.13 to a logic zero configures the PHY for 10 Mb/s operation. When Auto-Negotiation is disabled and bit 0.6 is set to a logic one, clearing bit 0.13 to a logic zero selects 1000 Mb/s operation. The combination of both bits 0.6 and 0.13 set to a logic one is reserved for future standardization. When Auto-Negotiation is enabled, bits 0.6 and 0.13 can be read or written, but the state of bits 0.6 and 0.13 have no effect on the link configuration, and it is not necessary for bits 0.6 and 0.13 to reflect the operating speed of the link when it is read. If a PHY reports via bits 1.15:9 and bits 15.15:12 that it is not able to operate at all speeds, the value of bits 0.6 and 0.13 shall correspond to a speed at which the PHY can operate, and any attempt to change the bits to an invalid setting shall be ignored.

The default value of bits 0.6 and 0.13 are the encoding of the highest data rate at which the PHY can operate as indicated by bits 1.15:9 and 15.15:12.

22.2.4.1.4 Auto-Negotiation enable

The Auto-Negotiation process shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13, 0.8, and 0.6 shall have no effect on the link configuration, and station operation other than that specified by the Auto-Negotiation protocol. If bit 0.12 is cleared to a logic zero, then bits 0.13, 0.8,

and 0.6 will determine the link configuration, regardless of the prior state of the link configuration and the Auto-Negotiation process.

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, the PHY shall return a value of zero in bit 0.12. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, bit 0.12 should always be written as zero, and any attempt to write a one to bit 0.12 shall be ignored.

The default value of bit 0.12 is one, unless the PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, in which case the default value of bit 0.12 is zero.

22.2.4.1.5 Power down

The PHY may be placed in a low-power consumption state by setting bit 0.11 to a logic one. Clearing bit 0.11 to zero allows normal operation. The specific behavior of a PHY in the power-down state is implementation specific. While in the power-down state, the PHY shall respond to management transactions. During the transition to the power-down state and while in the power-down state, the PHY shall not generate spurious signals on the MII or GMII.

A PHY is not required to meet the RX_CLK and TX_CLK signal functional requirements when either bit 0.11 or bit 0.10 is set to a logic one. A PHY shall meet the RX_CLK and TX_CLK signal functional requirements defined in 22.2.2 within 0.5 s after both bit 0.11 and 0.10 are cleared to zero.

The default value of bit 0.11 is zero.

22.2.4.1.6 Isolate

The PHY may be forced to electrically isolate its data paths from the MII or GMII by setting bit 0.10 to a logic one. Clearing bit 0.10 allows normal operation. When the PHY is isolated from the MII or GMII it shall not respond to the TXD data bundle, TX_EN, TX_ER and GTX_CLK inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD data bundle, COL, and CRS outputs. When the PHY is isolated from the MII or GMII it shall respond to management transactions.

A PHY that is connected to the MII via the mechanical interface defined in 22.6 shall have a default value of one for bit 0.10 so as to avoid the possibility of having multiple MII output drivers actively driving the same signal path simultaneously.

NOTE—This clause neither requires nor assumes any specific behavior at the MDI resulting from setting bit 0.10 to a logic one.

22.2.4.1.7 Restart Auto-Negotiation

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the PHY shall return a value of zero in bit 0.9. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, bit 0.9 should always be written as zero, and any attempt to write a one to bit 0.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 0.9 to a logic one. This bit is self-clearing, and a PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall not be affected by writing a zero to bit 0.9.

The default value of bit 0.9 is zero.

22.2.4.1.8 Duplex mode

The duplex mode can be selected via either the Auto-Negotiation process, or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled, setting bit 0.8 to a logic one configures the PHY for full duplex operation, and clearing bit 0.8 to a logic zero configures the PHY for half duplex operation. When Auto-Negotiation is enabled, bit 0.8 can be read or written, but the state of bit 0.8 has no effect on the link configuration. If a PHY reports via bits 1.15:9 and 15.15:12 that it is able to operate in only one duplex mode, the value of bit 0.8 shall correspond to the mode in which the PHY can operate, and any attempt to change the setting of bit 0.8 shall be ignored.

When a PHY is placed in the loopback mode of operation via bit 0.14, the behavior of the PHY shall not be affected by the state of bit 0.8.

The default value of bit 0.8 is zero, unless a PHY reports via bits 1.15:9 and 15.15:12 that it is able to operate only in full duplex mode, in which case the default value of bit 0.8 is one.

22.2.4.1.9 Collision test

The COL signal at the MII or GMII may be tested by setting bit 0.7 to a logic one. When bit 0.7 is set to one, the PHY shall assert the COL signal within 512 BT in response to the assertion of TX_EN. While bit 0.7 is set to one, the PHY shall de-assert the COL signal within 4 BT when connected to an MII, or 16 BT when connected to a GMII, in response to the de-assertion of TX_EN. Clearing bit 0.7 to zero allows normal operation.

The default value of bit 0.7 is zero.

NOTE—It is recommended that the Collision Test function be used only in conjunction with the loopback mode of operation defined in 22.2.4.1.2.

22.2.4.1.10 Speed selection

Bit 0.6 is used in conjunction with bits 0.13 and 0.12 to select the speed of operation as described in 22.2.4.1.3.

22.2.4.1.11 Reserved bits

Bits 0.4:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.1.12 Unidirectional enable

If a PHY reports via bit 1.7 that it lacks the ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established, the PHY shall return a value of zero in bit 0.5, and any attempt to write a one to bit 0.5 shall be ignored.

The ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established is controlled by bit 0.5 as well as the status of Auto-Negotiation Enable bit 0.12 and the Duplex Mode bit 0.8 as this ability can only be supported if Auto-Negotiation is disabled and the PHY is operating in full-duplex mode. If bit 0.5 is set to a logic one, bit 0.12 to logic zero and bit 0.8 to logic one, encoding and transmitting data from the media independent interface shall be enabled regardless of whether the PHY has determined that a valid link has been established. If bit 0.5 is set to a logic zero, bit 0.12 to logic one or bit 0.8 to logic zero, encoding and transmitting data from the

media independent interface shall be dependent on whether the PHY has determined that a valid link has been established. When bit 0.12 is one or bit 0.8 is zero, bit 0.5 shall be ignored.

A management entity shall set bit 0.5 to a logic one only after it has enabled an associated OAM sublayer (see Clause 57) or if this device is a 1000BASE-PX-D PHY. A management entity shall clear bit 0.5 to a logic zero prior to it disabling an associated OAM sublayer when this device is not a 1000BASE-PX-D PHY. To avoid collisions, a management entity should not set bit 0.5 of a 1000BASE-PX-U PHY to a logic one.

The default value of bit 0.5 is zero, except for 1000BASE-PX-D, where it is one.

22.2.4.2 Status register (Register 1)

The assignment of bits in the Status register is shown in Table 22–8. All of the bits in the Status register are read only, a write to the Status register shall have no effect.

Table 22–8—Status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex	1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X	RO
1.13	100BASE-X Half Duplex	1 = PHY able to perform half duplex 100BASE-X 0 = PHY not able to perform half duplex 100BASE-X	RO
1.12	10 Mb/s Full Duplex	1 = PHY able to operate at 10 Mb/s in full duplex mode 0 = PHY not able to operate at 10 Mb/s in full duplex mode	RO
1.11	10 Mb/s Half Duplex	1 = PHY able to operate at 10 Mb/s in half duplex mode 0 = PHY not able to operate at 10 Mb/s in half duplex mode	RO
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full duplex 100BASE-T2 0 = PHY not able to perform full duplex 100BASE-T2	RO
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half duplex 100BASE-T2	RO
1.8	Extended Status	1 = Extended status information in Register 15 0 = No extended status information in Register 15	RO
1.7	Unidirectional ability	1 = PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established	RO
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed. 0 = PHY will not accept management frames with preamble suppressed.	RO
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
1.4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO/ LH

Table 22–8—Status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
1.2	Link Status	1 = link is up 0 = link is down	RO/ LL
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/ LH
1.0	Extended Capability	1 = extended register capabilities 0 = basic register set capabilities only	RO

[a]RO = Read Only, LL = Latching Low, LH = Latching High

22.2.4.2.1 100BASE-T4 ability

When read as a logic one, bit 1.15 indicates that the PHY has the ability to perform link transmission and reception using the 100BASE-T4 signaling specification. When read as a logic zero, bit 1.15 indicates that the PHY lacks the ability to perform link transmission and reception using the 100BASE-T4 signaling specification.

22.2.4.2.2 100BASE-X full duplex ability

When read as a logic one, bit 1.14 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.14 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification.

22.2.4.2.3 100BASE-X half duplex ability

When read as a logic one, bit 1.13 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.13 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 100BASE-X signaling specification.

22.2.4.2.4 10 Mb/s full duplex ability

When read as a logic one, bit 1.12 indicates that the PHY has the ability to perform full duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.12 indicates that the PHY lacks the ability to perform full duplex link transmission and reception while operating at 10 Mb/s.

22.2.4.2.5 10 Mb/s half duplex ability

When read as a logic one, bit 1.11 indicates that the PHY has the ability to perform half duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.11 indicates that the PHY lacks the ability to perform half duplex link transmission and reception while operating at 10 Mb/s.

22.2.4.2.6 100BASE-T2 full duplex ability

When read as a logic one, bit 1.10 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 100BASE-T2 signaling specification. When read as a logic zero, bit 1.10 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-T2 signaling specification.

22.2.4.2.7 100BASE-T2 half duplex ability

When read as a logic one, bit 1.9 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 100BASE-T2 signaling specification. When read as a logic zero, bit 1.9 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 100BASE-T2 signaling specification.

22.2.4.2.8 Unidirectional ability

When read as a logic one, bit 1.7 indicates that the PHY has the ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.7 indicates the PHY is able to transmit data from the media independent interface only when the PHY has determined that a valid link has been established.

A PHY shall return a value of zero in bit 1.7 if it is not a 100BASE-X PHY using the PCS and PMA specified in 66.1 or a 1000BASE-X PHY using the PCS and PMA specified in 66.2.

22.2.4.2.9 MF preamble suppression ability

When read as a logic one, bit 1.6 indicates that the PHY is able to accept management frames regardless of whether they are or are not preceded by the preamble pattern described in 22.2.4.5.2. When read as a logic zero, bit 1.6 indicates that the PHY is not able to accept management frames unless they are preceded by the preamble pattern described in 22.2.4.5.2.

22.2.4.2.10 Auto-Negotiation complete

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the extended registers implemented by the Auto-Negotiation protocol (either Clause 28 or Clause 37) are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of the extended registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

22.2.4.2.11 Remote fault

When read as a logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

If a PHY has no provision for remote fault detection, it shall maintain bit 1.4 in a cleared state. Further information regarding the remote fault indication can be found in 37.2.1.5, 22.2.1.2, and 24.3.2.1.

22.2.4.2.12 Auto-Negotiation ability

When read as a logic one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

22.2.4.2.13 Link Status

When read as a logic one, bit 1.2 indicates that the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.2 indicates that the link is not valid. The criteria for determining link

validity is PHY specific. The Link Status bit shall be implemented with a latching function, such that the occurrence of a link failure condition will cause the Link Status bit to become cleared and remain cleared until it is read via the management interface. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

22.2.4.2.14 Jabber detect

When read as a logic one, bit 1.1 indicates that a jabber condition has been detected. This status indication is intended to support the management attribute defined in 30.5.1.1.6, aJabber, and the MAU notification defined in 30.5.1.3.1, nJabber. The criteria for the detection of a jabber condition is PHY specific. The Jabber Detect bit shall be implemented with a latching function, such that the occurrence of a jabber condition will cause the Jabber Detect bit to become set and remain set until it is cleared. The Jabber Detect bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

PHYs specified for 100 Mb/s operation or above do not incorporate a Jabber Detect function, as this function is defined to be performed in the repeater unit at these speeds. Therefore, PHYs specified for 100 Mb/s operation and above shall always return a value of zero in bit 1.1.

22.2.4.2.15 Extended capability

When read as a logic one, bit 1.0 indicates that the PHY provides an extended set of capabilities which may be accessed through the extended register set. When read as a logic zero, bit 1.0 indicates that the PHY provides only the basic register set.

22.2.4.2.16 Extended status

When read as a logic one, bit 1.8 indicates that the base register status information is extended into Register 15. All PHYs supporting 1000 Mb/s operation shall have this bit set to a logic one. When read as a logic zero, bit 1.8 indicates that the extended status is not implemented and that the PHY lacks the ability to perform transmission and reception at 1000 Mb/s.

22.2.4.3 Extended capability registers

In addition to the basic register set defined in 22.2.4.1 and 22.2.4.2, PHYs may provide an extended set of capabilities that may be accessed and controlled via the MII management interface. Thirteen registers have been defined within the extended address space for the purpose of providing a PHY-specific identifier to layer management, to provide control and monitoring for the Auto-Negotiation process, and to provide control and monitoring of power sourcing equipment, and to provide MDIO Manageable Device (MMD) register access.

If an attempt is made to perform a read transaction to a register in the extended register set, and the PHY being read does not implement the addressed register, the PHY shall not drive the MDIO line in response to the read transaction. If an attempt is made to perform a write transaction to a register in the extended register set, and the PHY being written does not implement the addressed register, the write transaction shall be ignored by the PHY.

22.2.4.3.1 PHY Identifier (Registers 2 and 3)

Registers 2 and 3 provide a 32-bit value, which shall constitute a unique identifier for a particular type of PHY. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier.

Bit 2.15 shall be the MSB of the PHY Identifier, and bit 3.0 shall be the LSB of the PHY Identifier.

The PHY Identifier shall be composed of the third through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the PHY manufacturer by the IEEE,[1] plus a six-bit manufacturer's model number, plus a four-bit manufacturer's revision number. The PHY Identifier is intended to provide sufficient information to support the oResourceTypeID object as required in 30.1.2.

The third bit of the OUI is assigned to bit 2.15, the fourth bit of the OUI is assigned to bit 2.14, and so on. Bit 2.0 contains the eighteenth bit of the OUI. Bit 3.15 contains the nineteenth bit of the OUI, and bit 3.10 contains the twenty-fourth bit of the OUI. Bit 3.9 contains the MSB of the manufacturer's model number. Bit 3.4 contains the LSB of the manufacturer's model number. Bit 3.3 contains the MSB of the manufacturer's revision number, and bit 3.0 contains the LSB of the manufacturer's revision number.

Figure 22–12 depicts the mapping of this information to the bits of Registers 2 and 3. Additional detail describing the format of OUIs can be found in IEEE Std 802.

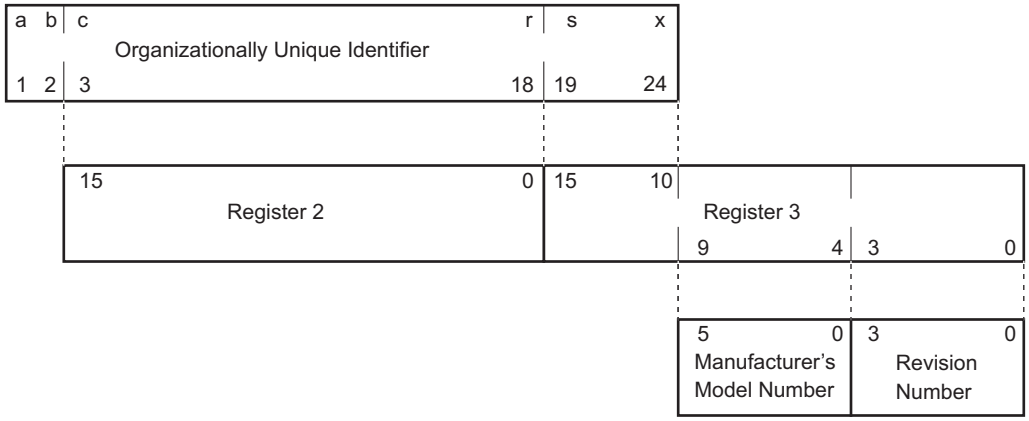

Figure 22–12—Format of PHY Identifier

22.2.4.3.2 Auto-Negotiation advertisement (Register 4)

Register 4 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.3 Auto-Negotiation link partner ability (Register 5)

Register 5 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.4 Auto-Negotiation expansion (Register 6)

Register 6 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.5 Auto-Negotiation next page (Register 7)

Register 7 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.6 Auto-Negotiation link partner Received Next Page (Register 8)

Register 8 provides 16 bits that are used by the Auto-Negotiation process. See 32.5.1 and 37.2.5.1.

[1]Interested applicants should contact the IEEE Standards Department, Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

22.2.4.3.7 MASTER-SLAVE control register (Register 9)

Register 9 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

22.2.4.3.8 MASTER-SLAVE status register (Register 10)

Register 10 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

22.2.4.3.9 PSE Control register (Register 11)

Register 11 provides control bits that are used by a PSE. See 33.6.1.1.

22.2.4.3.10 PSE Status register (Register 12)

Register 12 provides status bits that are supplied by a PSE. See 33.6.1.2.

22.2.4.3.11 MMD access control register (Register 13)

The assignment of bits in the MMD access control register is shown in Table 22–9. The MMD access control register is used in conjunction with the MMD access address data register (Register 14) to provide access to the MMD address space using the interface and mechanisms defined in 22.2.4.

Table 22–9—MMD access control register bit definitions

Bit(s)	Name	Description	R/W[a]
13.15:14	Function	13.1513.14 00= address 01= data, no post increment 10= data, post increment on reads and writes 11= data, post increment on writes only	R/W
13.13:5	Reserved	Write as 0, ignore on read	R/W
13.4:0	DEVAD	Device address	R/W

[a]R/W = Read/Write

Each MMD maintains its own individual address register as described in 45.2.7. The DEVAD field directs any accesses of Register 14 to the appropriate MMD as described in 45.2. If the access of Register 14 is an address access (bits 13.15:14 = 00) then it is directed to the address register within the MMD associated with the value in the DEVAD field (bits 13.4:0). Otherwise, both the DEVAD field and that MMD's address register direct the Register 14 data accesses to the appropriate registers within that MMD.

The Function field can be set to any of four values:

a) When set to 00, accesses to Register 14 access the MMD's individual address register. This address register should always be initialized before attempting any accesses to other MMD registers.
b) When set to 01, accesses to Register 14 access the register within the MMD selected by the value in the MMD's address register.

c) When set to 10, accesses to Register 14 access the register within the MMD selected by the value in the MMD's address register. After that access is complete, for both read and write accesses, the value in the MMD's address field is incremented.
d) When set to 11, accesses to Register 14 access the register within the MMD selected by the value in the MMD's address register. After that access is complete, for write accesses only, the value in the MMD's address field is incremented. For read accesses, the value in the MMD's address field is not modified.

For additional insight into the operation and usage of this register, see Annex 22D.

22.2.4.3.12 MMD access address data register (Register 14)

The assignment of bits in the MMD access address data register is shown in Table 22–10. The MMD access address data register is used in conjunction with the MMD access control register (Register 13) to provide access to the MMD address space using the interface and mechanisms defined in 22.2.4. Accesses to this register are controlled by the value of the fields in Register 13 and the contents of the MMD's individual address field as described in 22.2.4.3.11.

Table 22–10—MMD access address data register bit definitions

Bit(s)	Name	Description	R/W[a]
14.15:0	Address Data	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register	R/W

[a]R/W = Read/Write

For additional insight into the operation and usage of this register, see Annex 22D.

22.2.4.3.13 PHY specific registers

A particular PHY may provide additional registers beyond those defined above. Register addresses 16 through 31 (decimal) may be used to provide vendor-specific functions or abilities. The definition of Registers 4 through 14 are dependent on the version (Clause 28 or Clause 37) of Auto-Negotiation protocol used by the PHY.

22.2.4.4 Extended Status register (Register 15)

The Extended Status register is implemented for all PHYs capable of operation at speeds above 100 Mb/s. The assignment of bits in the Extended Status register is shown in Table 22–11 below. All of the bits in the Extended Status register are read only; a write to the Extended Status register shall have no effect.

22.2.4.4.1 1000BASE-X full duplex ability

When read as a logic one, bit 15.15 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification. When read as a logic zero, the bit 15.15 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification.

Table 22–11—Extended Status register bit definitions

Bit(s)	Name	Description	R/W[a]
15.15	1000BASE-X Full Duplex	1 = PHY able to perform full duplex 1000BASE-X 0 = PHY not able to perform full duplex 1000BASE-X	RO
15.14	1000BASE-X Half Duplex	1 = PHY able to perform half duplex 1000BASE-X 0 = PHY not able to perform half duplex 1000BASE-X	RO
15.13	1000BASE-T Full Duplex	1 = PHY able to perform full duplex 1000BASE-T 0 = PHY not able to perform full duplex 1000BASE-T	RO
15.12	1000BASE-T Half Duplex	1 = PHY able to perform half duplex 1000BASE-T 0 = PHY not able to perform half duplex 1000BASE-T	RO
15.11:0	Reserved	ignore when read	RO

[a]RO = Read Only

22.2.4.4.2 1000BASE-X half duplex ability

When read as a logic one, bit 15.14 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 1000BASE-X signaling specification. When read as a logic zero, the bit 15.14 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 1000BASE-X signaling specification.

22.2.4.4.3 1000BASE-T full duplex ability

When read as a logic one, bit 15.13 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 1000BASE-T signaling specification. When read as a logic zero, the bit 15.13 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 1000BASE-T signaling specification.

22.2.4.4.4 1000BASE-T half duplex ability

When read as a logic one, bit 15.12 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 1000BASE-T signaling specification. When read as a logic zero, the bit 15.12 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 1000BASE-T signaling specification.

22.2.4.4.5 Reserved bits

Bits 15:11:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.5 Management frame structure

Frames transmitted on the MII Management Interface shall have the frame structure shown in Table 22–12. The order of bit transmission shall be from left to right.

22.2.4.5.1 IDLE (IDLE condition)

The IDLE condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic one.

Table 22–12—Management frame format

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

22.2.4.5.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

If the STA determines that every PHY that is connected to the MDIO signal is able to accept management frames that are not preceded by the preamble pattern, then the STA may suppress the generation of the preamble pattern, and may initiate management frames with the ST (Start of Frame) pattern.

22.2.4.5.3 ST (start of frame)

The start of frame is indicated by a <01> pattern. This pattern assures transitions from the default logic one line state to zero and back to one.

22.2.4.5.4 OP (operation code)

The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.

22.2.4.5.5 PHYAD (PHY Address)

The PHY Address is five bits, allowing 32 unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address. A PHY that is connected to the station management entity via the mechanical interface defined in 22.6 shall always respond to transactions addressed to PHY Address zero <00000>. A station management entity that is attached to multiple PHYs must have prior knowledge of the appropriate PHY Address for each PHY.

22.2.4.5.6 REGAD (Register Address)

The Register Address is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address. The register accessed at Register Address zero <00000> shall be the control register defined in 22.2.4.1, and the register accessed at Register Address one <00001> shall be the status register defined in 22.2.4.2.

22.2.4.5.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY shall remain in a high-impedance state for the first bit time of the turnaround. The PHY shall drive a zero bit during the second bit time of the turnaround of a read transaction. During a write transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the

turnaround. Figure 22–13 shows the behavior of the MDIO signal during the turnaround field of a read transaction.

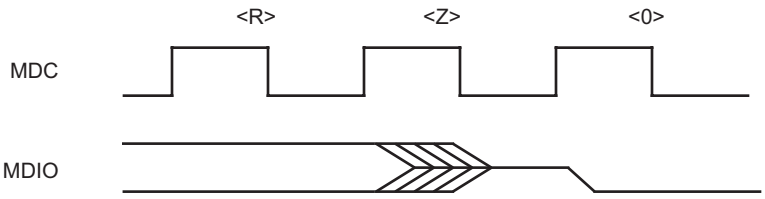

Figure 22–13—Behavior of MDIO during TA field of a read transaction

22.2.4.5.8 DATA (data)

The data field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.

22.3 Signal timing characteristics

All signal timing characteristics shall be measured using the techniques specified in Annex 22C. The signal threshold potentials $V_{ih(min)}$ and $V_{il(max)}$ are defined in 22.4.4.1.

The HIGH time of an MII signal is defined as the length of time that the potential of the signal is greater than or equal to $V_{ih(min)}$. The LOW time of an MII signal is defined as the length of time that the potential of the signal is less than or equal to $V_{il(max)}$.

The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

The propagation delay from an MII clock edge to a valid MII signal is defined as the length of time between when the clock exits the switching region and when the signal exits and remains out of the switching region.

22.3.1 Signals that are synchronous to TX_CLK

Figure 22–14 shows the timing relationship for the signals associated with the transmit data path at the MII connector. The clock to output delay shall be a minimum of 0 ns and a maximum of 25 ns.

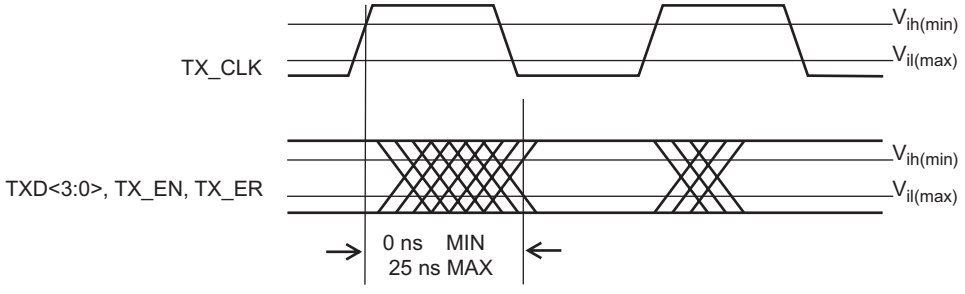

Figure 22–14—Transmit signal timing relationships at the MII

22.3.1.1 TX_EN

TX_EN is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as shown in Figure 22–14.

22.3.1.2 TXD<3:0>

TXD<3:0> is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as depicted in Figure 22–14.

22.3.1.3 TX_ER

TX_ER is transitioned synchronously with respect to the rising edge of TX_CLK as shown in Figure 22–14.

22.3.2 Signals that are synchronous to RX_CLK

Figure 22–15 shows the timing relationship for the signals associated with the receive data path at the MII connector. The timing is referenced to the rising edge of the RX_CLK. The input setup time shall be a minimum of 10 ns and the input hold time shall be a minimum of 10 ns.

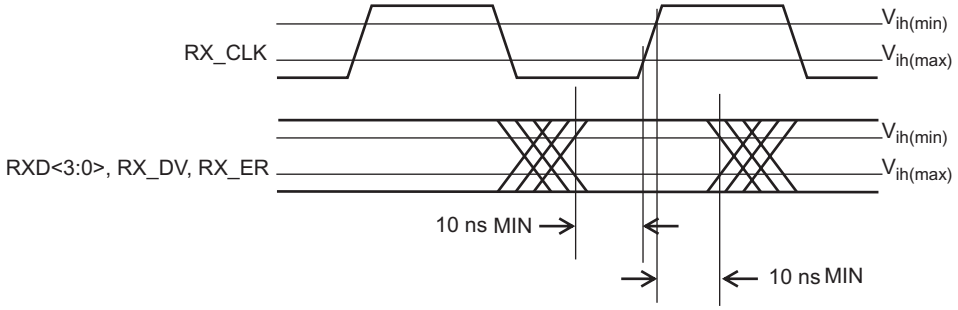

Figure 22–15—Receive signal timing relationships at the MII

22.3.2.1 RX_DV

RX_DV is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK with the timing shown in Figure 22–15.

22.3.2.2 RXD<3:0>

RXD<3:0> is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in Figure 22–15. The RXD<3:0> timing requirements must be met at all rising edges of RX_CLK.

22.3.2.3 RX_ER

RX_ER is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in Figure 22–15. The RX_ER timing requirements must be met at all rising edges of RX_CLK.

22.3.3 Signals that have no required clock relationship

22.3.3.1 CRS

CRS is driven by the PHY. Transitions on CRS have no required relationship to either of the clock signals provided at the MII.

22.3.3.2 COL

COL is driven by the PHY. Transitions on COL have no required relationship to either of the clock signals provided at the MII.

22.3.4 MDIO timing relationship to MDC

MDIO (Management Data Input/Output) is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the PHY. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 22–16, measured at the MII connector.

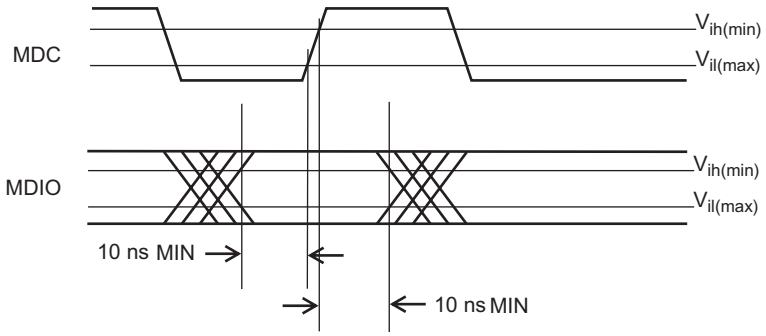

Figure 22–16—MDIO sourced by STA

When the MDIO signal is sourced by the PHY, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the PHY, as measured at the MII connector, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 22–17.

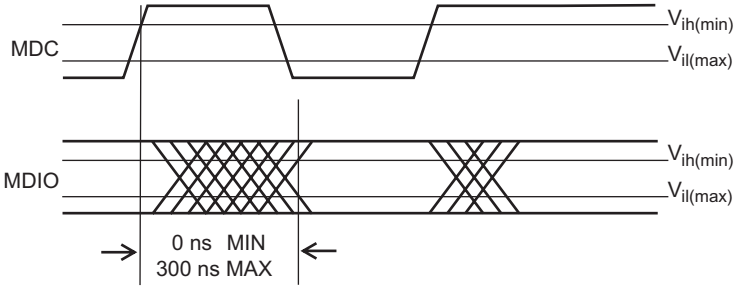

Figure 22–17—MDIO sourced by PHY

22.4 Electrical characteristics

The electrical characteristics of the MII are specified such that the three application environments described in 22.1 are accommodated. The electrical specifications are optimized for the integrated circuit to integrated circuit application environment, but integrated circuit drivers and receivers that are implemented in compliance with the specification will also support the mother board to daughter board and short cable application environments, provided those environments are constrained to the limits specified in this clause.

NOTE—The specifications for the driver and receiver characteristics can be met with TTL compatible input and output buffers implemented in a digital CMOS ASIC process.

22.4.1 Signal levels

The MII uses TTL signal levels, which are compatible with devices operating at a nominal supply voltage of either 5.0 or 3.3 V.

NOTE—Care should be taken to ensure that all MII receivers can tolerate dc input potentials from 0.00 V to 5.50 V, referenced to the COMMON signal, and transient input potentials as high as 7.3 V, or as low as –1.8 V, referenced to the COMMON signal, which can occur when MII signals change state. The transient duration will not exceed 15 ns. The dc source impedance will be no less than $R_{oh(min)}$. The transient source impedance will be no less than (68 × 0.85 =) 57.8 Ω.

22.4.2 Signal paths

MII signals can be divided into two groups: signals that go between the STA and the PHY, and signals that go between the Reconciliation sublayer and the PHY.

Signals between the STA and the PHY may connect to one or more PHYs. When a signal goes between the STA and a single PHY, the signal's path is a point-to-point transmission path. When a signal goes between the STA and multiple PHYs, the signal's transmission path has drivers and receivers attached in any order along the length of the path and is not considered a point-to-point transmission path.

Signals between the Reconciliation sublayer and the PHY may also connect to one or more PHYs. However, the transmission path of each of these signals shall be either a point-to-point transmission path or a sequence of point-to-point transmission paths connected in series.

All connections to a point-to-point transmission path are at the path ends. The simplest point-to-point transmission path has a driver at one end and a receiver at the other. Point-to-point transmission paths can also have more than one driver and more than one receiver if the drivers and receivers are lumped at the ends of the path, and if the maximum propagation delay between the drivers and receivers at a given end of the path is a very small fraction of the 10%–90% rise/fall time for signals driven onto the path.

The MII shall use unbalanced signal transmission paths. The characteristic impedance Z_o of transmission paths is not specified for electrically short paths where transmission line reflections can be safely ignored.

The characteristic impedance Z_o of electrically long transmission paths or path segments shall be 68 Ω ± 15%.

The output impedance of the driver shall be used to control transmission line reflections on all electrically long point-to-point signal paths.

NOTE—In the context of this clause, a transmission path whose round-trip propagation delay is less than half of the 10%–90% rise/fall time of signals driven onto the path is considered an electrically short transmission path.

22.4.3 Driver characteristics

The driver characteristics defined in this clause apply to all MII signal drivers. The driver characteristics are specified in terms of both their ac and dc characteristics.

NOTE—Rail-to-rail drivers that comply with the driver output V-I diagrams in Annex 22B will meet the following ac and dc characteristics.

22.4.3.1 DC characteristics

The high (one) logic level output potential V_{oh} shall be no less than 2.40 V at an output current I_{oh} of –4.0 mA. The low (zero) logic level output potential V_{ol} shall not be greater than 0.40 V at an output current I_{ol} of 4.0 mA.

22.4.3.2 AC characteristics

Drivers must also meet certain ac specifications in order to ensure adequate signal quality for electrically long point-to-point transmission paths. The ac specifications shall guarantee the following performance requirements.

The initial incident potential change arriving at the receiving end of a point-to-point MII signal path plus its reflection from the receiving end of the path must switch the receiver input potential monotonically from a valid high (one) level to $V_{il} \leq V_{il(max)} - 200$ mV, or from a valid low (zero) level to $V_{ih} \geq V_{ih(min)} + 200$ mV.

Subsequent incident potential changes arriving at the receiving end of a point-to-point MII signal path plus their reflections from the receiving end of the path must not cause the receiver input potential to reenter the range $V_{il(max)} - 200\ mV < V_i < V_{ih(min)} + 200$ mV except when switching from one valid logic level to the other. Such subsequent incident potential changes result from a mismatch between the characteristic impedance of the signal path and the driver output impedance.

22.4.4 Receiver characteristics

The receiver characteristics are specified in terms of the threshold levels for the logical high (one) and logical low (zero) states. In addition, receivers must meet the input current and capacitance limits.

22.4.4.1 Voltage thresholds

An input potential V_i of 2.00 V or greater shall be interpreted by the receiver as a logical high (one). Thus, $V_{ih(min)} = 2.00$ V. An input potential V_i of 0.80 V or less shall be interpreted by the receiver as a logical low (zero). Thus, $V_{il(max)} = 0.80$ V. The switching region is defined as signal potentials greater than $V_{il(max)}$ and less than $V_{ih(min)}$. When the input signal potential is in the switching region, the receiver output is undefined.

22.4.4.2 Input current

The input current requirements shall be measured at the MII connector and shall be referenced to the +5 V supply and COMMON pins of the connector. The input current requirements shall be met across the full range of supply voltage specified in 22.5.1.

The bidirectional signal MDIO has two sets of input current requirements. The MDIO drivers must be disabled when the input current measurement is made.

The input current characteristics for all MII signals shall fall within the limits specified in Table 22–13.

Table 22–13—Input current limits

Symbol	Parameter	Condition	Signal(s)	Min (µA)	Max (µA)
I_{ih}	Input high current	V_i=5.25 V	All except COL, MDC, MDIO[a]	—	200
			COL[b]	—	20
			MDC[c]	—	20
			MDIO[d]	—	3000
			MDIO[e]	—	20
I_{il}	Input low current	V_i=0.00 V	All except COL, MDC, MDIO[a]	–20	—
			COL[b]	–200	—
			MDC[c]	–20	—
			MDIO[d]	–180	—
			MDIO[e]	–3800	—
I_{iq}	Input quiescent current	V_i=2.4 V	MDIO[d]	—	1450
			MDIO[e]	–1450	—

[a]Measured at input of Reconciliation sublayer for CRS, RXD<3:0>, RX_CLK, RX_DV, RX_ER, and TX_CLK. Measured at inputs of PHY for TXD<3:0>, TX_EN, and TX_ER.
[b]Measured at input of Reconciliation sublayer.
[c]Measured at input of PHY.
[d]Measured at input of STA.
[e]Measured at input of PHY, which can be attached via the mechanical interface specified in 22.6.

NOTE—These limits for dc input current allow the use of weak resistive pull-ups or pull-downs on the input of each MII signal. They allow the use of weak resistive pull-downs on the signals other than COL, MDC, and MDIO. They allow the use of a weak resistive pull-up on the signal COL. They allow the use of a resistive pull-down of 2 kΩ ± 5% on the MDIO signal in the STA. They require a resistive pull-up of 1.5 kΩ ± 5% on the MDIO signal in a PHY that is attached to the MII via the mechanical interface specified in 22.6. The limits on MDC and MDIO allow the signals to be “bused” to several PHYs that are contained on the same printed circuit assembly, with a single PHY attached via the MII connector.

22.4.4.3 Input capacitance

For all signals other than MDIO, the receiver input capacitance C_i shall not exceed 8 pF.

For the MDIO signal, the transceiver input capacitance shall not exceed 10 pF.

22.4.5 Cable characteristics

The MII cable consists of a bundle of individual twisted pairs of conductors with an overall shield covering this bundle. Each twisted pair shall be composed of a conductor for an individual signal and a return path dedicated to that signal.

NOTE—It is recommended that the signals RX_CLK and TX_CLK be connected to pairs that are located in the center of the cable bundle.

22.4.5.1 Conductor size

The specifications for dc resistance in 22.4.5.6 and characteristic impedance in 22.4.5.2 assume a conductor size of 0.32 mm (28 AWG).

22.4.5.2 Characteristic impedance

The single-ended characteristic impedance of each twisted pair shall be 68 Ω ± 10%. The characteristic impedance measurement shall be performed with the return conductor connected to the cable's overall shield at both ends of the cable.

22.4.5.3 Delay

The propagation delay for each twisted pair, measured from the MII connector to the PHY, shall not exceed 2.5 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable. The propagation delay shall be measured at a frequency of 25 MHz.

22.4.5.4 Delay variation

The variation in the propagation delay of the twisted pairs in a given cable bundle, measured from the MII connector to the PHY, shall not exceed 0.1 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable.

22.4.5.5 Shielding

The overall shield must provide sufficient shielding to meet the requirements of protection against electromagnetic interference.

The overall shield shall be terminated to the connector shell as defined in 22.6.2. A double shield, consisting of both braid and foil shielding, is strongly recommended.

22.4.5.6 DC resistance

The dc resistance of each conductor in the cable, including the contact resistance of the connector, shall not exceed 150 mΩ measured from the MII connector to the remote PHY.

22.4.6 Hot insertion and removal

The insertion or removal of a PHY from the MII with power applied (hot insertion or removal) shall not damage the devices on either side of the MII. In order to prevent contention between multiple output buffers driving the PHY output signals, a PHY that is attached to the MII via the mechanical interface defined in 22.6 shall ensure that its output buffers present a high impedance to the MII during the insertion process, and shall ensure that this condition persists until the output buffers are enabled via the Isolate control bit in the management interface basic register.

NOTE—The act of inserting or removing a PHY from an operational system may cause the loss of one or more packets or management frames that may be in transit across the MII or MDI.

22.5 Power supply

When the mechanical interface defined in 22.6 is used to interconnect printed circuit subassemblies, the Reconciliation sublayer shall provide a regulated power supply for use by the PHY.

The power supply shall use the following MII lines:

+5 V: The plus voltage output to the PHY.
COMMON: The return to the power supply.

22.5.1 Supply voltage

The regulated supply voltage to the PHY shall be 5 Vdc ± 5% at the MII connector with respect to the COMMON circuit at the MII over the range of load current from 0 to 750 mA. The method of over/under voltage protection is not specified; however, under no conditions of operation shall the source apply a voltage to the +5 V circuit of less than 0 V or greater than +5.25 Vdc.

Implementations that provide a conversion from the MII to the Attachment Unit Interface (AUI) to support connection to 10 Mb/s Medium Attachment Units (MAUs) will require a supplemental power source in order to meet the AUI power supply requirements specified in 7.5.2.5.

22.5.2 Load current

The sum of the currents carried on the +5 V lines shall not exceed 750 mA, measured at the MII connector. The surge current drawn by the PHY shall not exceed 5 A peak for a period of 10 ms. The PHY shall be capable of powering up from 750 mA current limited sources.

22.5.3 Short-circuit protection

Adequate provisions shall be made to ensure protection of the power supply from overload conditions, including a short circuit between the +5 V lines and the COMMON lines.

22.6 Mechanical characteristics

When the MII is used to interconnect two printed circuit assemblies via a short length of cable, the cable shall be connected to the circuit assembly that implements the Reconciliation sublayer by means of the mechanical interface defined in this clause.

22.6.1 Definition of mechanical interface

A 40-pole connector having the mechanical mateability dimensions as specified in IEC 61076-3-101: 1997 shall be used for the MII connector. The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall have a female connector with screw locks, and the mating cable shall have a male connector with jack screws.

No requirements are imposed on the mechanical interface used to connect the MII cable to the PHY circuit assembly when the MII cable is permanently attached to the PHY circuit assembly, as shown in Figure 22–2. If the cable is not permanently attached to the PHY circuit assembly, then a male connector with jack screws shall be used for the MII connector at the PHY circuit assembly.

NOTE—All MII conformance tests are performed at the mating surfaces of the MII connector at the Reconciliation sublayer end of the cable. If a PHY circuit assembly does not have a permanently attached cable, the vendor must ensure that all of the requirements of this clause are also met when a cable that meets the requirements of 22.4.5 is used to attach the PHY circuit assembly to the circuit assembly that contains the Reconciliation sublayer.

22.6.2 Shielding effectiveness and transfer impedance

The shells of these connectors shall be plated with conductive material to ensure the integrity of the current path from the cable shield to the chassis. The transfer impedance of this path shall not exceed the values listed in Table 22–14, after a minimum of 500 cycles of mating and unmating. The shield transfer impedance values listed in the table are measured in accordance with the procedure defined in Annex L of IEEE Std 1394-1995 [B33][2].

Table 22–14—Transfer impedance performance requirements

Frequency	Value
30 MHz	–26 dBΩ
159 MHz	–13 dBΩ
500 MHz	–5 dBΩ

All additions to provide for female shell to male shell conductivity shall be on the shell of the connector with male contacts. There should be multiple contact points around the sides of this shell to provide for shield continuity.

22.6.3 Connector pin numbering

Figure 22–18 depicts the MII connector pin numbering, as seen looking into the contacts of a female connector from the mating side.

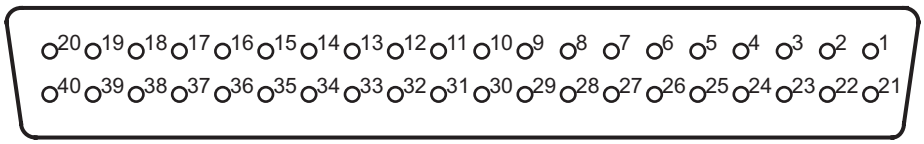

Figure 22–18—MII connector pin numbering

22.6.4 Clearance dimensions

The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall provide sufficient clearance around the MII connector to allow the attachment of cables that use die cast metal backshells and overmold assemblies. This requirement may be met by providing the clearance dimensions shown in Figure 22–19.

[2]The numbers in brackets correspond to those of the bibliography in Annex A in Section One of this standard.

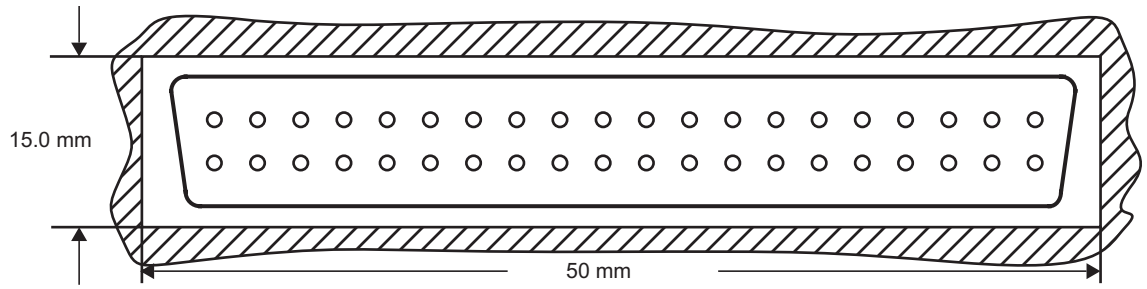

Figure 22–19—MII connector clearance dimensions

22.6.5 Contact assignments

Table 22–15 shows the assignment of circuits to connector contacts.

Table 22–15—MII connector contact assignments

Contact	Signal name	Contact	Signal name
1	+5 V	21	+5 V
2	MDIO	22	COMMON
3	MDC	23	COMMON
4	RXD<3>	24	COMMON
5	RXD<2>	25	COMMON
6	RXD<1>	26	COMMON
7	RXD<0>	27	COMMON
8	RX_DV	28	COMMON
9	RX_CLK	29	COMMON
10	RX_ER	30	COMMON
11	TX_ER	31	COMMON
12	TX_CLK	32	COMMON
13	TX_EN	33	COMMON
14	TXD<0>	34	COMMON
15	TXD<1>	35	COMMON
16	TXD<2>	36	COMMON
17	TXD<3>	37	COMMON
18	COL	38	COMMON
19	CRS	39	COMMON
20	+5 V	40	+5 V

22.7 Protocol implementation conformance statement (PICS) proforma for Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[3]

22.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

22.7.2 Identification

22.7.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

22.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2005, Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required?No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2005.)	

Date of Statement	

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

22.7.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*GM	Implementation of GMII	22.2.4	O		
*MUNI	Implementation of unidirectional PCS	22.2.4	O		

22.7.3 PICS proforma tables for reconciliation sublayer and media independent interface

22.7.3.1 Mapping of PLS service primitives

Item	Feature	Subclause	Status	Support	Value/Comment
PL1	Response to RX_ER	22.2.1.5	M		Must produce FrameCheckError at MAC

22.7.3.2 MII signal functional specifications

Item	Feature	Subclause	Status	Support	Value/Comment
SF1	TX_CLK frequency	22.2.2.1	M		25% of transmitted data rate (25 MHz or 2.5 MHz)
SF2	TX_CLK duty cycle	22.2.2.1	M		35% to 65%
SF3	RX_CLK min high/low time	22.2.2.2	M		35% of nominal period
SF4	RX_CLK synchronous to recovered data	22.2.2.2	M		
SF5	RX_CLK frequency	22.2.2.2	M		25% of received data rate (25 MHz or 2.5 MHz)
SF6	RX_CLK duty cycle	22.2.2.2	M		35% to 65%
SF7	RX_CLK source due to loss of signal	22.2.2.2	M		Nominal clock reference (e.g., TX_CLK reference)
SF8	RX_CLK transitions only while RX_DV de-asserted	22.2.2.2	M		
SF9	RX_CLK max high/low time following de-assertion of RX_DV	22.2.2.2	M		max 2 times the nominal period
SF10	TX_EN assertion	22.2.2.3	M		On first nibble of preamble
SF11	TX_EN remains asserted	22.2.2.3	M		Stay asserted while all nibbles are transmitted over MII
SF12	TX_EN transitions	22.2.2.3	M		Synchronous with TX_CLK
SF13	TX_EN negation	22.2.2.3	M		Before first TX_CLK after final nibble of frame
SF14	TXD<3:0> transitions	22.2.2.4	M		Synchronous with TX_CLK

22.7.3.2 MII signal functional specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
SF15	TXD<3:0> effect on PHY while TX_EN is de-asserted	22.2.2.4	M		No effect
SF16	TX_ER transitions	22.2.2.5	M		Synchronous with TX_CLK
SF17	TX_ER effect on PHY while TX_EN is asserted	22.2.2.5	M		Cause PHY to emit invalid symbol
SF18	TX_ER effect on PHY while operating at 10 Mb/s, or when TX_EN is de-asserted	22.2.2.5	M		No effect on PHY
SF19	TX_ER implementation	22.2.2.5	M		At MII of a PHY
SF20	TX_ER pulled down if not actively driven	22.2.2.5	M		At MII of a repeater or MAC/RS only
SF21	RX_DV transitions	22.2.2.6	M		Synchronous with RX_CLK
SF22	RX_DV assertion	22.2.2.6	M		From first recovered nibble to final nibble of a frame per Figure 22–6
SF23	RX_DV negation	22.2.2.6	M		Before the first RX_CLK follows the final nibble per Figure 22–6
SF24	RXD<3:0> effect on Reconciliation sublayer while RX_DV is de-asserted	22.2.2.7	M		No effect
SF25	RX_ER assertion	22.2.2.8	M		By PHY to indicate error
SF26	RX_ER transitions	22.2.2.8	M		Synchronous with RX_CLK
SF27	RX_ER effect on Reconciliation sublayer while RX_DV is de-asserted	22.2.2.8	M		No effect
SF28	CRS assertion	22.2.2.9	M		By PHY when either transmit or receive is NON-IDLE
SF29	CRS de-assertion	22.2.2.9	M		By PHY when both transmit and receive are IDLE
SF30	CRS assertion during collision	22.2.2.9	M		Remain asserted throughout
SF31	COL assertion	22.2.2.10	M		By PHY upon detection of collision on medium
SF32	COL remains asserted while collision persists	22.2.2.10	M		
SF33	COL response to SQE	22.2.2.10	M		Assertion by PHY
SF34	MDC min high/low time	22.2.2.11	M		160 ns
SF35	MDC min period	22.2.2.11	M		400 ns
SF36	MDIO uses three-state drivers	22.2.2.12	M		
SF37	PHY pull-up on MDIO	22.2.2.12	M		1.5 kΩ ± 5% (to +5 V)
SF38	STA pull-down on MDIO	22.2.2.12	M		2 kΩ ± 5% (to 0 V)

22.7.3.3 Frame structure

Item	Feature	Subclause	Status	Support	Value/Comment
FS1	Format of transmitted frames	22.2.3	M		Per Figure 22–10
FS2	Nibble transmission order	22.2.3	M		Per Figure 22–11
FS3	Preamble 7 octets long	22.2.3.2.1	M		10101010 10101010 10101010 10101010 10101010 10101010 10101010
FS4	Preamble and SFD transmission	22.2.3.2.1	M		Per Table 22–3
FS5	Preamble and SFD reception	22.2.3.2.2	M		Per Table 22–4, Table 22–5
FS6	N octets transmitted as 2N nibbles	22.2.3.3	M		Per Figure 22–11
FS7	Indication of excess nibbles	22.2.3.5	M		Frame contains non-integer number of octets is received

22.7.3.4 Management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Incorporate of basic register set	22.2.4	M		Two 16-bit registers as Control register (Register 0) and Status register (Register 1)
MF2	Action on reset	22.2.4.1.1	M		Reset the entire PHY including Control and Status to default value and set bit 0.15 = 1
MF3	Return 1 until reset completed	22.2.4.1.1	M		Yes (when reset is done, 0.15 is self clearing)
MF4	Reset completes within 0.5 s	22.2.4.1.1	M		
MF5	Loopback mode	22.2.4.1.2	M		Whenever 0.14 is 1
MF6	Receive circuitry isolated from network in loopback mode	22.2.4.1.2	M		
MF7	Effect of assertion of TX_EN in loopback mode	22.2.4.1.2	M		No transmission
MF8	Propagation of data in loop-back mode	22.2.4.1.2	M		PHY accepts transmit data and return it as receive data
MF9	Delay from TX_EN to RX_DV in loopback mode	22.2.4.1.2	M		Less than 512 BT
MF10	Behavior of COL in loopback mode	22.2.4.1.2	M		De-asserted (for 0.7 = 0)
MF11	Behavior of COL in loopback mode	22.2.4.1.2	M		If 0.7 = 1, see MF33 and MF34
MF12	Value of speed selection bits	22.2.4.1.3	M		Set to match a valid PHY speed

22.7.3.4 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF13	Ignore writes to speed selection bits for unsupported speed	22.2.4.1.3	M		
MF14	Auto-Negotiation enable	22.2.4.1.4	M		By setting 0.12 = 1
MF15	Duplex mode, speed selection have no effect when Auto-Negotiation is enabled	22.2.4.1.4	M		If 0.12=1, bits 0.13, 0.8 and 0.6 have no effect on link configuration
MF16	PHY without Auto-Negotiation returns value of zero	22.2.4.1.4	M		Yes (if 1.3=0, then 0.12=0)
MF17	PHY without Auto-Negotiation ignores writes to enable bit	22.2.4.1.4	M		Yes (if 1.3=0, 0.12 always = 0 and cannot be changed)
MF18	Response to management transactions in power down	22.2.4.1.5	M		Remains active
MF19	Spurious signals in power down	22.2.4.1.5	M		None (not allowed)
MF20	TX_CLK and RX_CLK stabilize within 0.5 s	22.2.4.1.5	M		Yes (after both bits 0.11 and 0.10 are cleared to zero)
MF21	PHY Response to input signals while isolated	22.2.4.1.6	M		NONE
MF22	High impedance on PHY output signals while isolated	22.2.4.1.6	M		Yes (TX_CLK, RX_CLK, RX_DV, RX_ER, RXD bundle, COL, and CRS)
MF23	Response to management transactions while isolated	22.2.4.1.6	M		Remains active
MF24	Default value of isolate	22.2.4.1.6	M		0.10 =1
MF25	PHY without Auto-Negotiation returns value of zero	22.2.4.1.7	M		0.9 = 0 if 1.3 = 0 or 0.12 = 0
MF26	PHY without Auto-Negotiation ignores writes to restart bit	22.2.4.1.7	M		0.9 = 0, cannot be changed if 1.3 = 0 or 0.12 = 0
MF27	Restart Auto-Negotiation	22.2.4.1.7	M		When 0.9 = 1 if 0.12 = 1 and 1.3 = 1
MF28	Return 1 until Auto-Negotiation initiated	22.2.4.1.7	M		0.9 is self clearing to 0
MF29	Auto-Negotiation not effected by clearing bit	22.2.4.1.7	M		
MF30	Value of duplex mode bit for PHYs with one duplex mode	22.2.4.1.8	M		Set 0.8 to match the correct PHY duplex mode
MF31	PHY with one duplex mode ignores writes to duplex bit	22.2.4.1.8	M		Yes (0.8 remains unchanged)
MF32	Loopback not affected by duplex mode	22.2.4.1.8	M		Yes (0.8 has no effect on PHY when 0.14 = 1)
MF33	Assertion of COL in collision test mode	22.2.4.1.9	M		Within 512 BT after TX_EN is asserted

22.7.3.4 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF34	De-assertion of COL in collision test mode	22.2.4.1.9	M		After TX_EN is de-asserted within: MII = 4 BT, GMII = 16 BT
MF35	Reserved bits written as zero	22.2.4.1.11	M		
MF36	Reserved bits ignored when read	22.2.4.1.11	M		
MF37	PHY returns 0 in reserved bits	22.2.4.1.11	M		
MF38	PHY without unidirectional ability	22.2.4.1.12	M		PHY returns a value of 0 in 0.5 if 1.7=0
MF39	PHY without unidirectional ability	22.2.4.1.12	M		PHY always maintains a value of 0 in 0.5 if 1.7=0
MF40	Unidirectional enable	22.2.4.1.12	MUNI:M		By setting 0.12 = 0, 0.8 = 1 and 0.5 = 1
MF41	Unidirectional disable	22.2.4.1.12	MUNI:M		By setting 0.12 = 1, 0.8 = 0 or 0.5 = 0
MF42	Ignore bit 0.5	22.2.4.1.12	MUNI:M		Ignore 0.5 when 0.12 = 1 or 0.8 = 0
MF43	Enable unidirectional mode	22.2.4.1.12	MUNI:M		Enable only when OAM sub-layer is enabled or when part of 1000BASE-PX-D PHY
MF44	Disable unidirectional mode	22.2.4.1.12	MUNI:M		Unidirectional mode is disabled before disabling OAM sublayer when not part of 1000BASE-PX-D PHY
MF45	Unidirectional ability	22.2.4.2.8	M		Bit 1.7 = 0 for all PHYs except those using 66.1 and 66.2
MF46	Effect of write on status register	22.2.4.2	M		No effect
MF47	Reserved bits ignored when read	22.2.4.2.8	M		
MF48	PHY returns 0 in reserved bits	22.2.4.2.8	M		
MF49	PHY returns 0 if Auto-Negotiation disabled	22.2.4.2.10	M		Yes (1.5 = 0 when 0.12 = 0)
MF50	PHY returns 0 if it lacks ability to perform Auto-Negotiation	22.2.4.2.10	M		Yes (1.5 = 0 when 1.3 = 0)
MF51	Remote fault has latching function	22.2.4.2.11	M		Yes (once set will remain set until cleared)
MF52	Remote fault cleared on read	22.2.4.2.11	M		Yes
MF53	Remote fault cleared on reset	22.2.4.2.11	M		Yes (when 0.15 = 1)
MF54	PHY without remote fault returns value of zero	22.2.4.2.11	M		Yes (1.4 always 0)

22.7.3.4 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF55	Link status has latching function	22.2.4.2.13	M		Yes (once cleared by link failure will remain cleared until read by MII)
MF56	Jabber detect has latching function	22.2.4.2.14	M		Yes (once set will remain set until cleared)
MF57	Jabber detect cleared on read	22.2.4.2.14	M		
MF58	Jabber detect cleared on reset	22.2.4.2.14	M		
MF59	All PHYs operating at rates of 100 Mb/s or above return 0 for jabber detect	22.2.4.2.14	M		Yes (1.1 always = 0 for all PHYs operating at rates of 100 Mb/s or above)
MF60	MDIO not driven if register read is unimplemented	22.2.4.3	M		Yes (MDIO remain high impedance)
MF61	Write has no effect if register written is unimplemented	22.2.4.3	M		
MF62	Registers 2 and 3 constitute unique identifier for PHY type	22.2.4.3.1	M		
MF63	MSB of PHY identifier is 2.15	22.2.4.3.1	M		
MF64	LSB of PHY identifier is 3.0	22.2.4.3.1	M		
MF65	Composition of PHY identifier	22.2.4.3.1	O		22-bit OUI, 6-bit model, 4-bit version per Figure 22–12
MF66	Format of management frames	22.2.4.5	M		Per Table 22–11
MF67	Idle condition on MDIO	22.2.4.5.1	M		High impedance state
MF68	MDIO preamble sent by STA	22.2.4.5.2	M		32 contiguous logic one bits
MF69	MDIO preamble observed by PHY	22.2.4.5.2	M		32 contiguous logic one bits
MF70	Assignment of PHYAD 0	22.2.4.5.5	M		Address of PHY attached via Mechanical Interface
MF71	Assignment of REGAD 0	22.2.4.5.6	M		MII control register address
MF72	Assignment of REGAD 1	22.2.4.5.6	M		MII status register address
MF73	High impedance during first bit time of turnaround in read transaction	22.2.4.5.7	M		

22.7.3.4 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF74	PHY drives zero during second bit time of turnaround in read transaction	22.2.4.5.7	M		
MF75	STA drives MDIO during turnaround in write transaction	22.2.4.5.7	M		
MF76	First data bit transmitted	22.2.4.5.8	M		Bit 15 of the register being addressed
MF77	Incorporate Extended Status register	22.2.4	GM:M		16-bit register Extended Status register (Register 15)
MF78	Reserved bits written as zero	22.2.4.2.8	GM:M		
MF79	Extended Status	22.2.4.2.16	GM:M		Yes (1.8 always = 1 for 1000 Mb/s operation)
MF80	Write to Extended Status register	22.2.4.4	GM:M		No effect
MF81	Reserved bits written as zero	22.2.4.4.5	GM:M		
MF82	Reserved bits ignored when read	22.2.4.4.5	GM:M		
MF83	PHY returns 0 in reserved bits	22.2.4.4.5	GM:M		

22.7.3.5 Signal timing characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
ST1	Timing characteristics measured in accordance with Annex 22C	22.3	M		
ST2	Transmit signal clock to output delay	22.3.1	M		Min = 0 ns; Max = 25 ns per Figure 22–14
ST3	Receive signal setup time	22.3.2	M		Min = 10 ns per Figure 22–15
ST4	Receive signal hold time	22.3.2	M		Min = 10 ns per Figure 22–15
ST5	MDIO setup and hold time	22.3.4	M		Setup min = 10 ns; Hold min = 10 ns per Figure 22–16
ST6	MDIO clock to output delay	22.3.4	M		Min = 0 ns; Max = 300 ns per Figure 22–17

22.7.3.6 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
EC1	Signal paths are either point to point, or a sequence of point-to-point transmission paths	22.4.2	M		
EC2	MII uses unbalanced signal transmission paths	22.4.2	M		
EC3	Characteristic impedance of electrically long paths	22.4.2	M		68 Ω ± 15%
EC4	Output impedance of driver used to control reflections	22.4.2	M		On all electrically long point to point signal paths
EC5	V_{oh}	22.4.3.1	M		≥ 2.4 V (I_{oh} = –4 mA)
EC6	V_{ol}	22.4.3.1	M		≤ 0.4 V (I_{ol} = 4 mA)
EC7	Performance requirements to be guaranteed by ac specifications	22.4.3.2	M		Min switching potential change (including its reflection) ≥ 1.8 V
EC8	$V_{ih(min)}$	22.4.4.1	M		2 V
EC9	$V_{il(max)}$	22.4.4.1	M		0.8 V
EC10	Input current measurement point	22.4.4.2	M		At MII connector
EC11	Input current reference potentials	22.4.4.2	M		Reference to MII connector +5 V and COMMON pins
EC12	Input current reference potential range	22.4.4.2	M		0 V to 5.25 V
EC13	Input current limits	22.4.4.2	M		Per Table 22–12
EC14	Input capacitance for signals other than MDIO	22.4.4.3	M		≤ 8 pF
EC15	Input capacitance for MDIO	22.4.4.3	M		≤ 10 pF
EC16	Twisted-pair composition	22.4.5	M		Conductor for each signal with dedicated return path
EC17	Single-ended characteristic impedance	22.4.5.2	M		68 Ω ± 10%
EC18	Characteristic impedance measurement method	22.4.5.2	M		With return conductor connected to cable shield

22.7.3.6 Electrical characteristics *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
EC19	Twisted-pair propagation delay	22.4.5.3	M		≤ 2.5 ns
EC20	Twisted-pair propagation delay measurement method	22.4.5.3	M		With return conductor connected to cable shield
EC21	Twisted-pair propagation delay measurement frequency	22.4.5.3	M		25 MHz
EC22	Twisted-pair propagation delay variation	22.4.5.4	M		≤ 0.1 ns
EC23	Twisted-pair propagation delay variation measurement method	22.4.5.4	M		With return conductor connected to cable shield
EC24	Cable shield termination	22.4.5.5	M		To the connector shell
EC25	Cable conductor DC resistance	22.4.5.6	M		≤ 150 mΩ
EC26	Effect of hot insertion/removal	22.4.6	M		Causes no damage
EC27	State of PHY output buffers during hot insertion	22.4.6	M		High impedance
EC28	State of PHY output buffers after hot insertion	22.4.6	M		High impedance until enabled via Isolate bit

22.7.3.7 Power supply

Item	Feature	Subclause	Status	Support	Value/Comment
PS1	Regulated power supply provided	22.5	M		To PHY by Reconciliation sublayer
PS2	Power supply lines	22.5	M		+5 V and COMMON (return of +5 V)
PS3	Regulated supply voltage limits	22.5.1	M		5 Vdc ± 5%
PS4	Over/under voltage limits	22.5.1	M		Over limit = 5.25 Vdc Under limit = 0 V
PS5	Load current limit	22.5.2	M		750 mA
PS6	Surge current limit	22.5.2	M		≤ 5 A peak for 10 ms
PS7	PHY can power up from current limited source	22.5.2	M		From 750 mA current limited source
PS8	Short-circuit protection	22.5.2	M		When +5 V and COMMON are shorted

22.7.3.8 Mechanical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
*MC1	Use of Mechanical Interface	22.6	O		Optional
MC2	Connector reference standard	22.6.1	MC1:M		IEC 61076-3-101: 1997
MC3	Use of female connector	22.6.1	MC1:M		At MAC/RS side
MC4	Use of male connector	22.6.1	MC1:M		At PHY mating cable side
MC5	Connector shell plating	22.6.2	MC1:M		Use conductive material
MC6	Shield transfer impedance	22.6.2	MC1:M		After 500 cycles of mating/ unmating, per Table 22–13
MC7	Additions to provide for female shell to male shell conductivity	22.6.2	MC1:M		On shell of conductor with male contacts
MC8	Clearance dimensions	22.6.4	MC1:M		15 mm × 50 mm, per Figure 22–19