STM32H7- PWR

Power Controller

Revision 1.0

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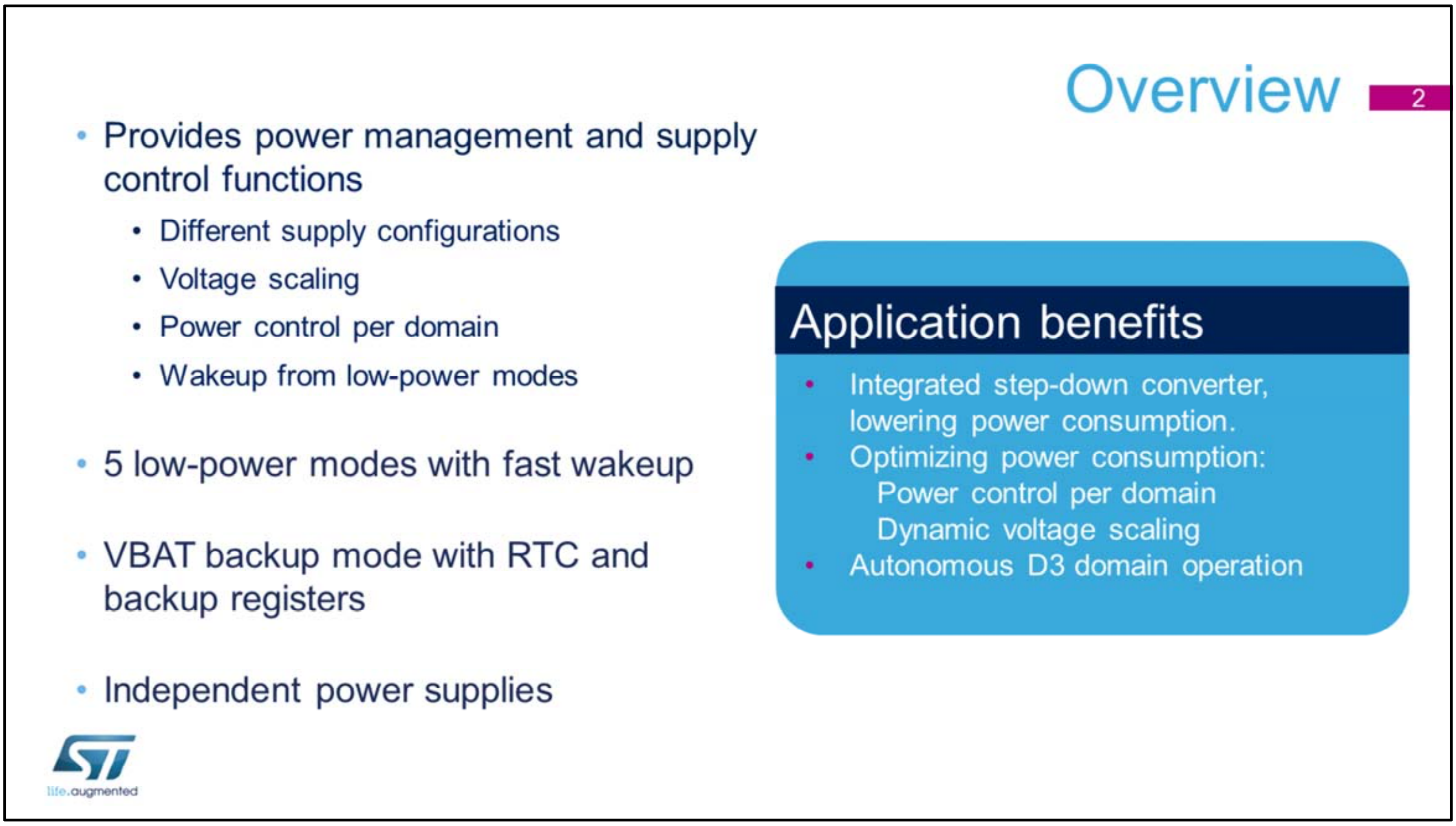
Hello, and welcome to this presentation of the STM32H7 power controller. The STM32H7's power management functions and all power modes will also be covered in this presentation.



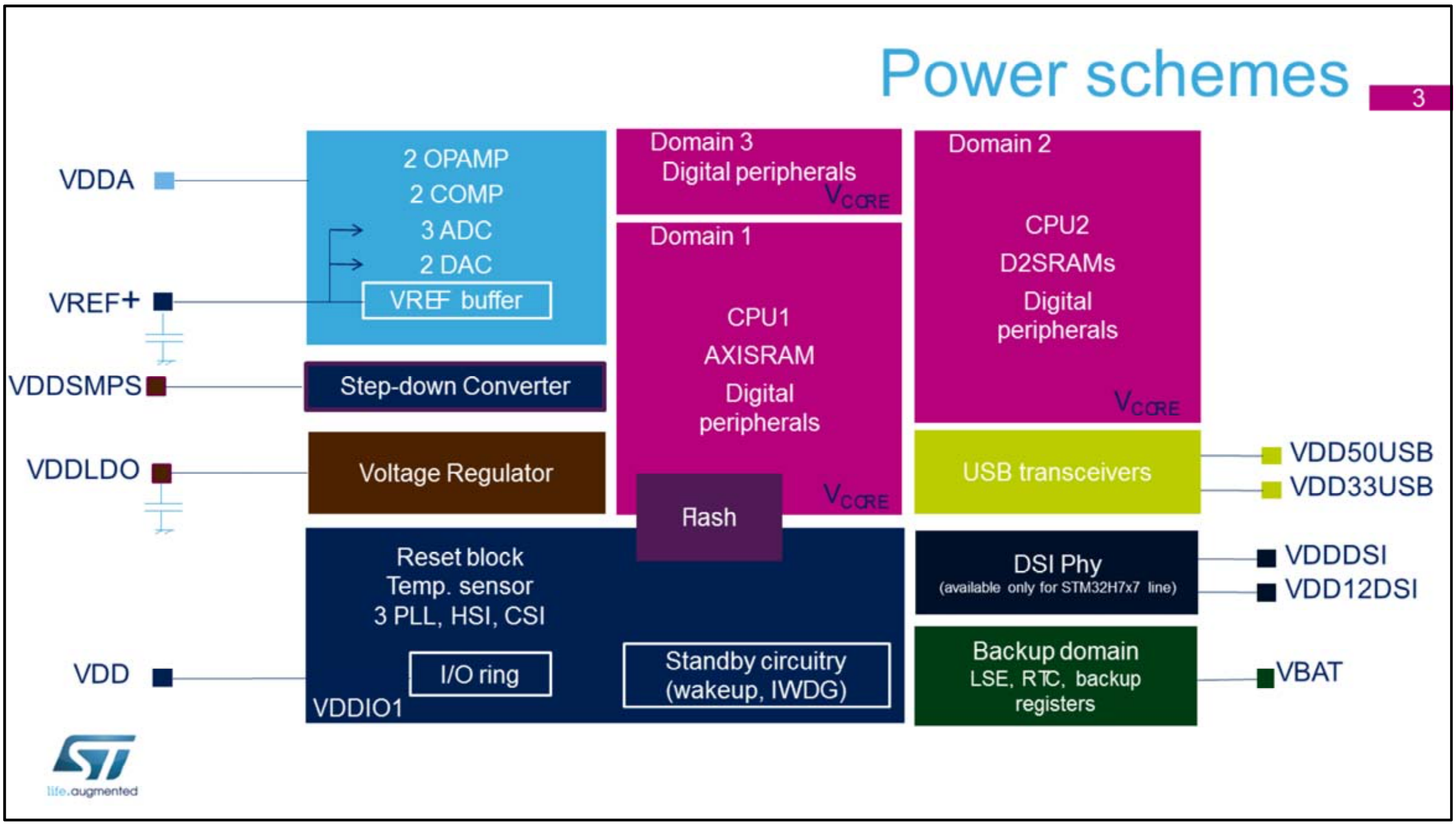
The STM32H7 has several key features related to power management including several low-power modes, where it is still possible to wake up the MCU with an event on an I/O as well as a large number of peripherals that can wake up from the various low-power modes.

The D3 autonomous mode allows transfer of data on communication peripherals without waking up the CPUs.

Several power supplies are independent, allowing reduction of the MCU power consumption while some peripherals are supplied at higher voltages.

Thanks to the large number of power modes and independent power domains, STM32H7 devices offer high flexibility to minimize the power consumption and adjust it depending on active peripherals, required performance and needed wake-up sources.

The integrated step-down converter reduces STM32H7 power consumption at minimal cost.



STM32H7 devices have several independent power supplies, which can be set at different voltages or tied together. The main power supply is VDD, supplying almost all I/Os except for some IOs of Ports A, C, and B. VDD also supplies the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog. VDD supplies the step-down converter which may directly provide the VCORE supply. VCORE supplies the 3 Domains (CPU1 Cortex-M7, CPU2 Cortex-M4 and D3 domain) with most of the digital peripherals and the SRAMs. The Flash memory is supplied by both VCORE and VDD.
VCORE may be supplied through the voltage regulator which is supplied on VDDLDO.
The STM32H7 features several independent supplies for peripherals: VDDA for the analog peripherals, VDD50USB and VDD33USB for the USB transceiver, VDDDSI and VDD12DSI for the DSI Physical layer. The VREF+ pin

provides the reference voltage to the analog-to-digital and to digital-to-analog converters and can be used as an external buffer reference for the application.
A backup battery can be connected to the VBAT pin to supply the backup domain.

Power schemes

Optimized power and performance thanks to independent power supplies

- V_{DD} from 1.71 to 3.6 V (1.62 to 3.6V with external supply supervisor)
- V_{BAT} from 1.2 to 3.6V including the RTC and 128-byte backup registers
- V_{DDSMPS} from 1.62 to 3.6 V
- V_{DDLDO} from 1.62 to 3.6 V ($V_{DDLDO} \leq V_{DD}$)
- V_{DDA} from 1.62 to 3.6 V →
  - 1.62 V min. when ADCs or COMPs are used
  - 1.8 V when DACs are used
  - 2.0 V when op amps are used
  - 1.8 V min. when V_{REFBUF} is used
- $V_{DD50USB}$ from 4.5 to 5.5 V for USB regulator
- $V_{DD33USB}$ from 3 to 3.6 V for USB transceivers
- V_{DDDSI} from 3 to 3.6 V for DSI regulator
- $V_{DD12DSI}$ from 1.2V for DSI Physical layer

(V_{DDDSI} and $V_{DD12DSI}$: available only for STM32H7x7 line)

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The main power supply VDD ensures full featured operation in all power modes from 1.71 up to 3.6 V, allowing to be supplied by an external 1.8 V regulator. Device functionality is guaranteed down to 1.62 V, the minimum voltage after which a brown-out reset is generated. Other independent supplies are provided for peripherals operating at a different voltage.

The analog power supply VDDA can be connected to any voltage other than VDD. When the analog-to-digital converters or comparators are used, the VDDA voltage must be greater than 1.62 V. When the digital-to-analog converters or comparators are used, VDDA must be greater than 1.8 V. When operational amplifiers are used, VDD must be greater than 2.0 V.

The USB regulator supplied from VDD50USB at 5 V generates the USB power supply VDD33USB. When the USB is used, VDD33USB must be greater than 3 V.

The DSI regulator supplied from VDDDSI greater than 1.62V generates the DSI power supply VDD12DSI. When the DSI is used, VDD12DSI must be greater than 1.2 V.

A backup domain is supplied by VBAT, which must be greater than 1.2 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the 128-byte backup registers.

Power schemes

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Independent voltage reference supplies for analog performance

- V_{REF+} : reference voltage for ADCs and DACs
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer.
  - VREF+ pin, and thus the internal voltage reference, is not available on the TFBGA100 package. On this package, this pin is double-bonded with V_{DDA} which can be connected to an external reference. With this configuration, the internal voltage reference buffer is not available.

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The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer. This allows the converters performance to be improved by providing an isolated and independent reference voltage.

Supply configurations

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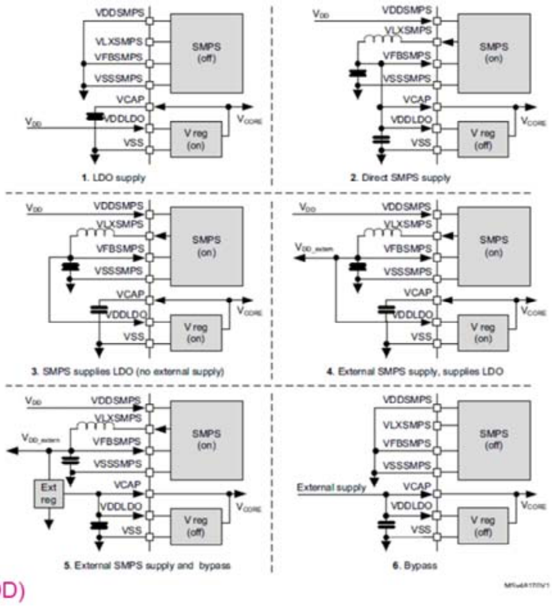
Flexible selection between performance and cost

- Core supply from SD convertor and/or Voltage regulator
  - 1. LDO Supply (SD disabled)
    - LDO supplied from same supply as VDD
  - 2. Direct SD Supply (LDO disabled)
    - Regulator follows device operation modes
  - 3. SD supplies LDO (No external supply)
    - Both regulators follow device operation modes
  - 4. SD external supply, supplies LDO
    - SD is forced on in high performance mode
    - LDO follow device operation modes
  - 5. SD external supply & LDO bypass (LDO disabled)
    - SD is forced on in high performance mode
  - 6. Bypass (SD & LDO disabled)



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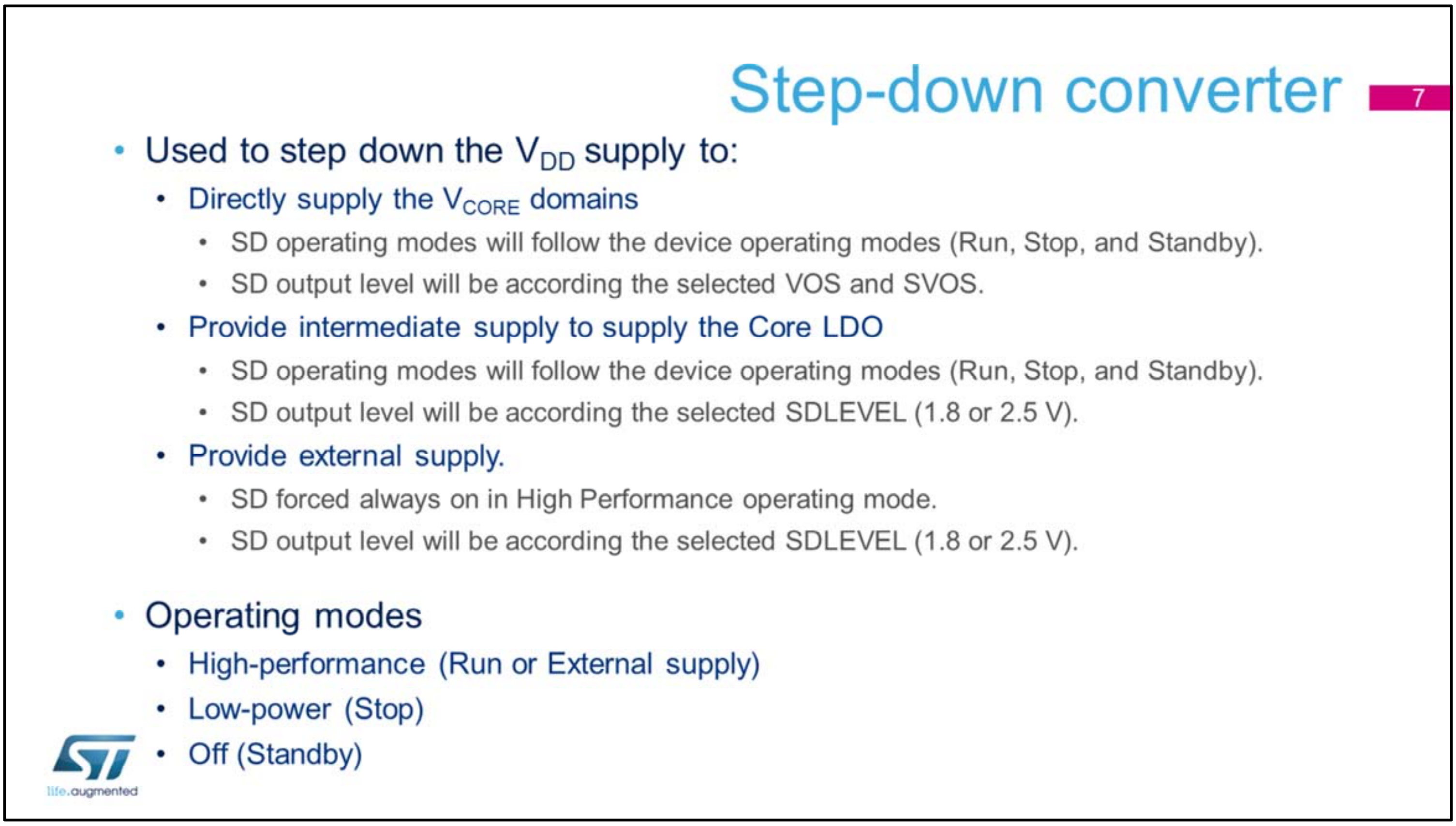
(SD can't be used to supply VDD)

The SMPS step-down convertor (SD convertor) can be used in 3 different modes or disabled:
1 – Directly supply the VCORE domain as shown in Configuration 2. This offers the lowest power consumption.
2 – Used to supply the voltage regulator at an intermediate supply level, as shown in Configuration 3. This offers low power consumption with a low noise VCORE supply.
3 – Used to supply external circuitry, as shown in Configurations 4 and 5. In this case, the voltage regulator can still be supplied from the same external supply provided by the step-down convertor.
4 – Disabled, as shown in Configurations 1 and 6. This offers a low-cost solution at higher power consumption rates.
At STM32H7 startup, the supply configuration is programmed in PWR controller's CR3 register. This register is "write once" to protect against accidental over-writes.

The step-down convertor cannot be used to supply the

STM32H7's VDD supply, but can be used to supply the VDDIO2 supply.



When directly supplying the V_{CORE} domain, the step-down convertor provides the supply level according to VOS and SVOS scaling. The step-down converter’s operating mode follows the device’s modes.

When used to supply the voltage regulator, the step-down convertor may provide an intermediate voltage at 1.8 or 2.5 V. The step-down converter’s operating mode follows the device’s modes.

When the step-down converter is used to supply external circuitry, it may provide a voltage at 1.8 or 2.5 V. In this case, the operating modes are fixed to “High Performance”.

LDO regulator

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- Used to regulate the V_{DDLDO} supply to the V_{CORE} level
  - Directly supply the V_{CORE} domains
    - LDO operating modes will follow the device operating modes (Run, Stop, and Standby).
    - LDO output level will be according the selected VOS and SVOS.
  - Bypass
    - LDO is off, the Core domain is directly supplied on V_{CORE}.
- Operating modes
    - Main (Run)
    - Low-power (Stop)
    - Off (Standby)

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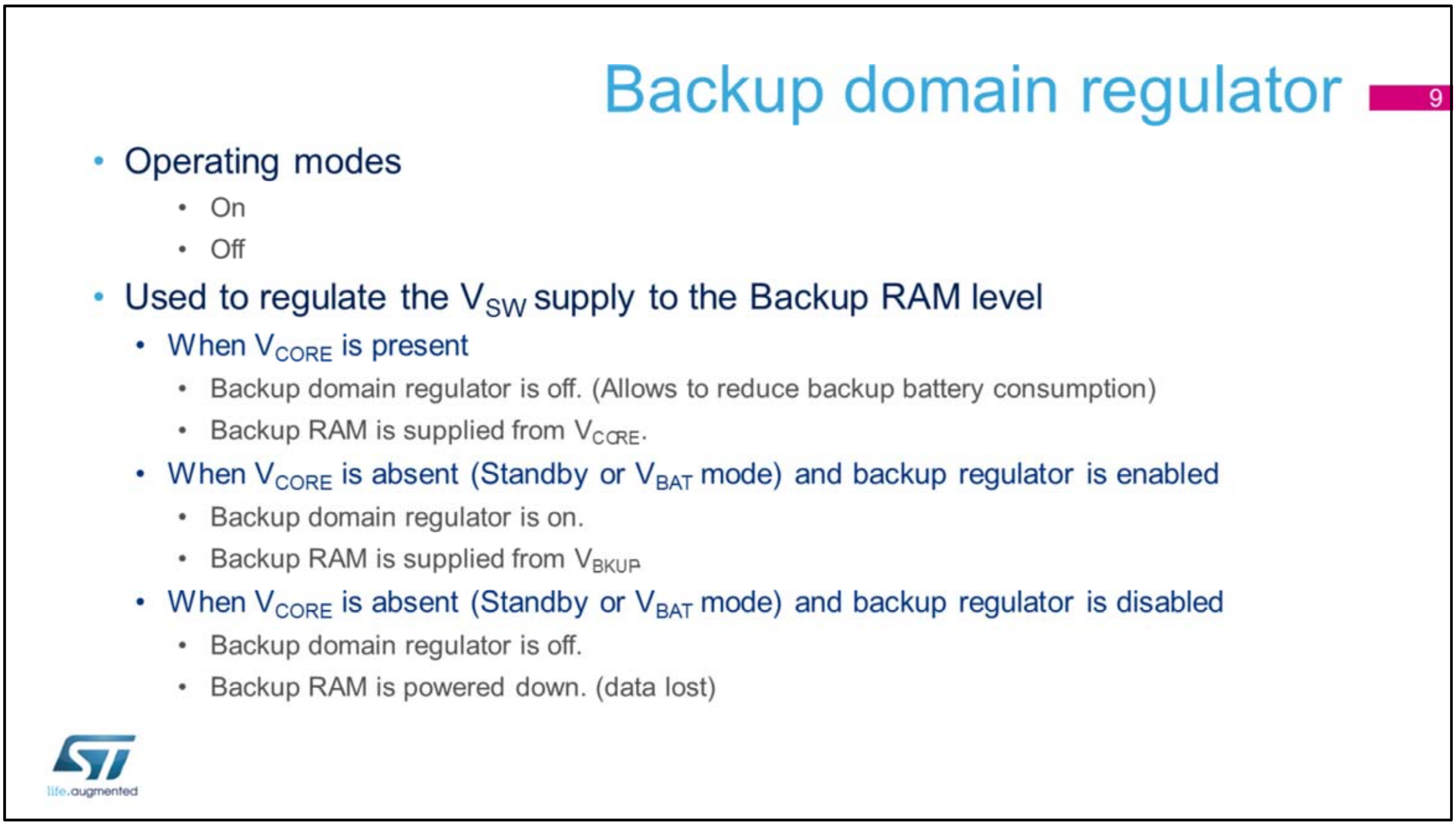
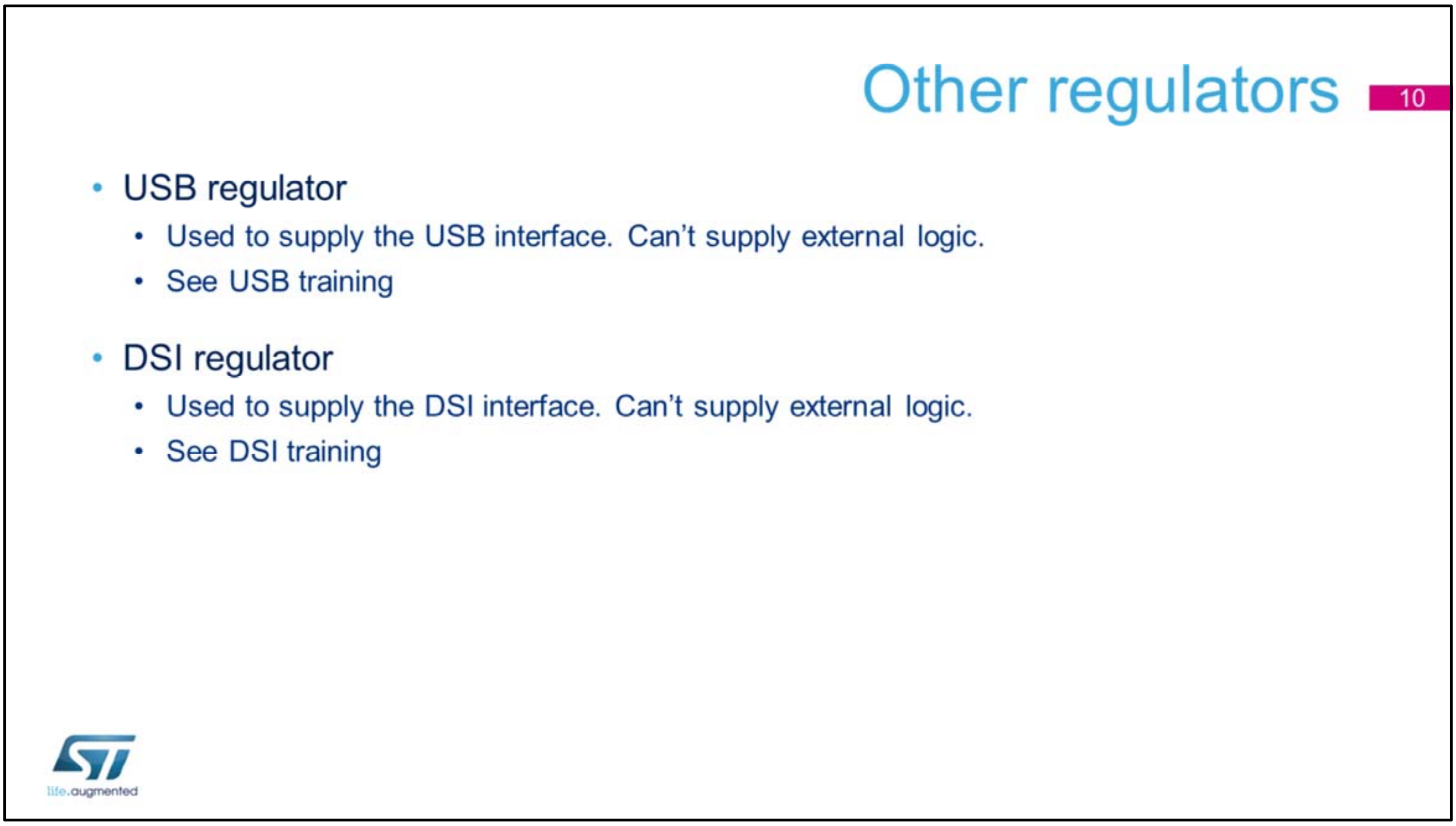
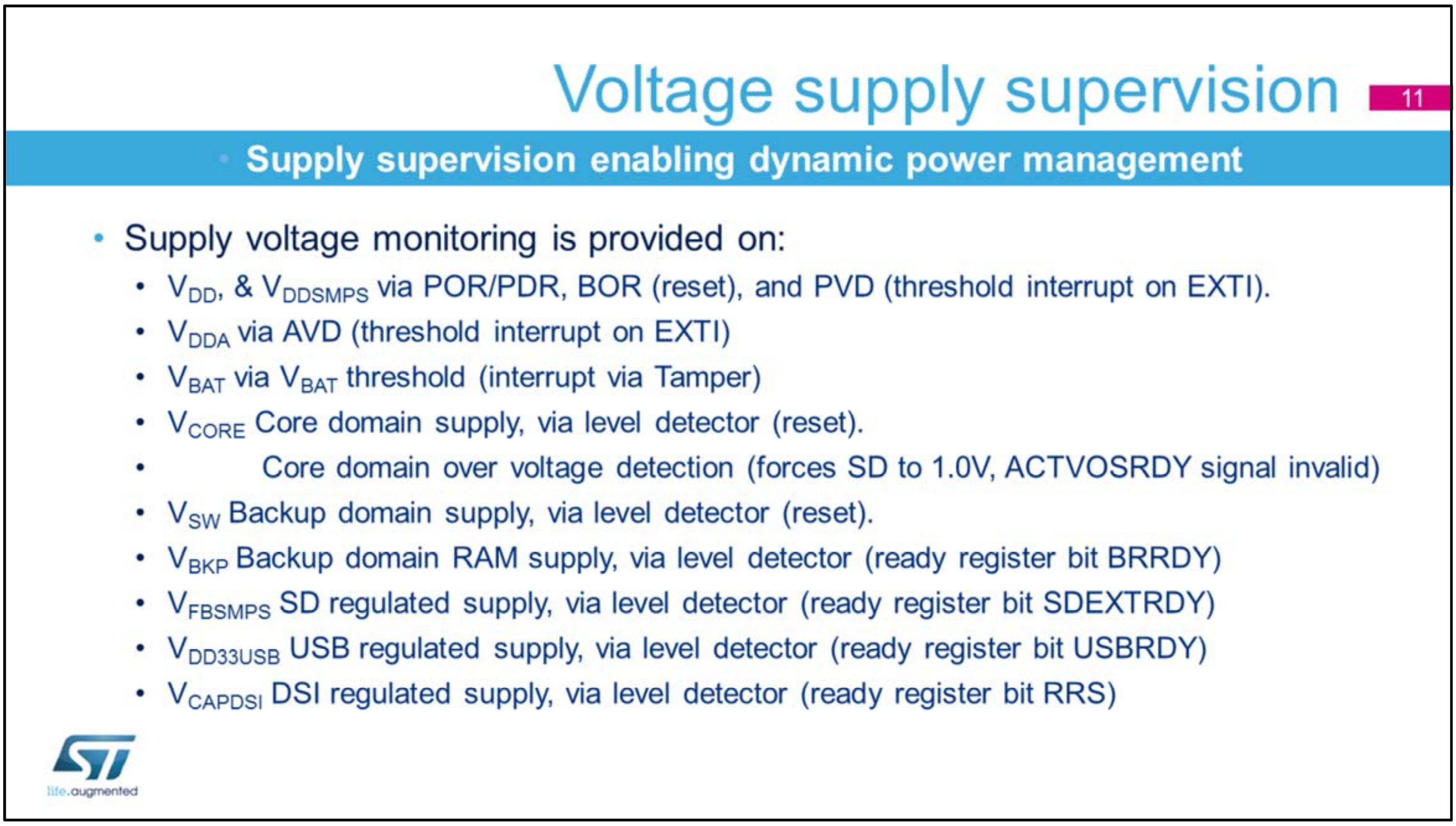
When used, the voltage regulator provides the VCORE supply level according to VOS and SVOS scaling. The voltage regulator’s operating mode follows the device’s modes.
When the VCORE is supplied from another supply, the voltage regulator is placed in bypassed mode.



The Backup regulator is used to keep the context of the Backup RAM in STANDBY and VBAT modes. The backup regulator is enabled by the BREN bit in PWR register CR2 and checks its readiness before entering STANDBY or VBAT mode.



An independent USB regulator generates the $V_{DD33USB}$ from a 5V supply.



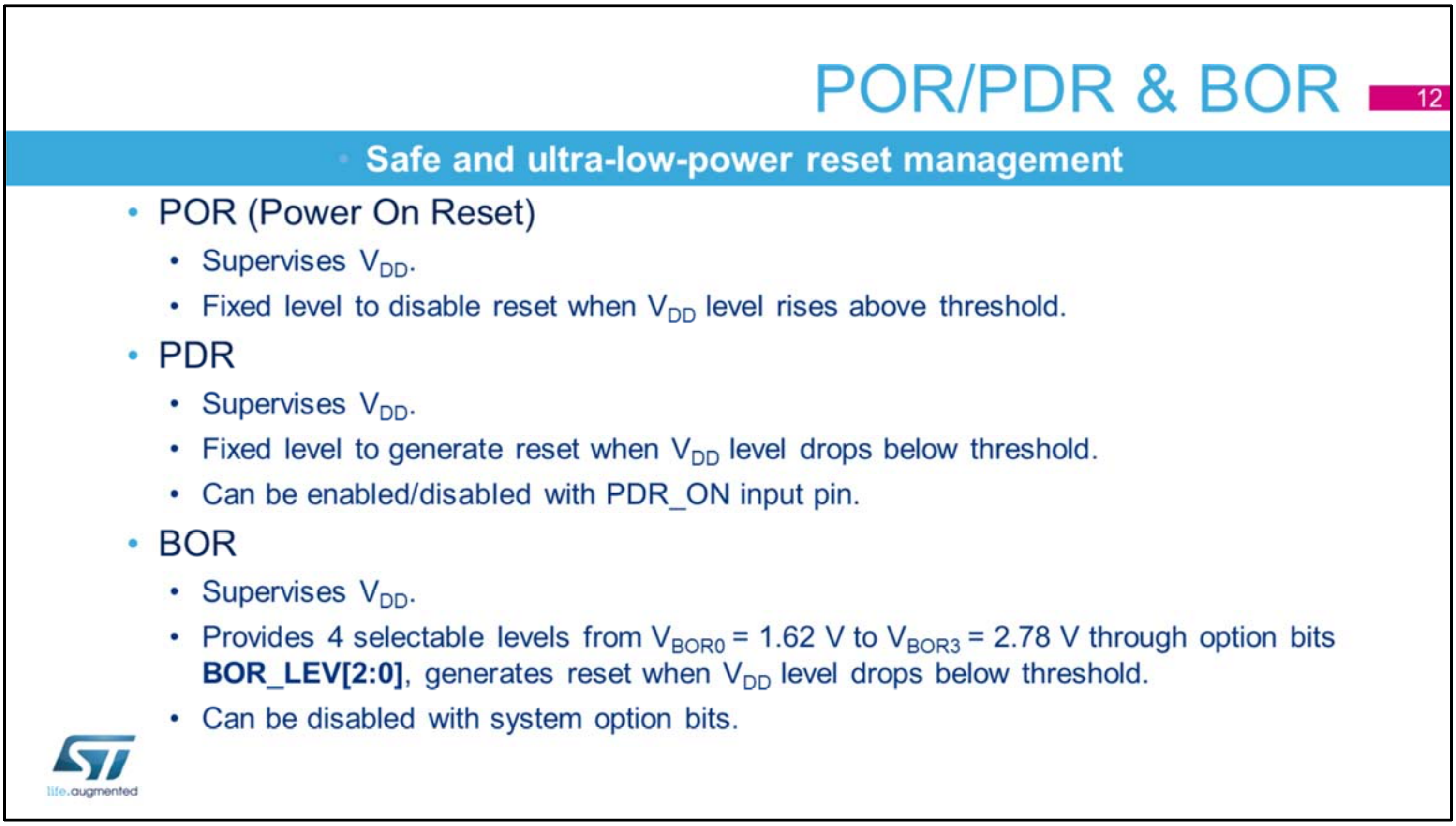
The power supply supervisor ensures dynamic power supply management.

STM32H7 devices embed power management on main VDD, analog VDDA, VBAT supply input, VCORE domain, Backup VSW domain, Backup regulator VBKP supply, step-down convertor VFBSMPS, USB interface VDD33USB supply and DSI VCAPDSI supplies.

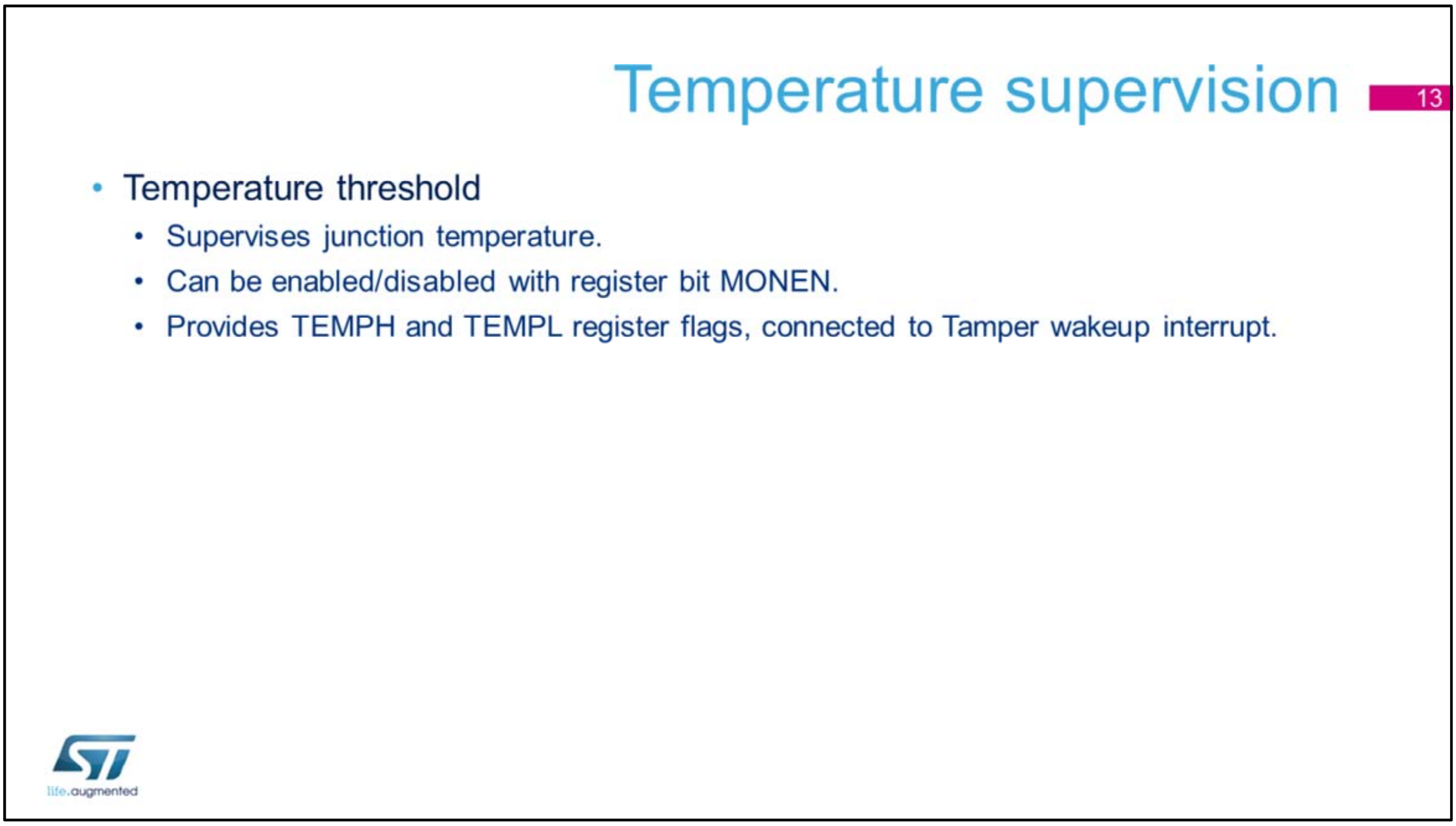
The main VDD supervisor handles reset management and voltage detection via the programmable voltage detector (PVD) when VDD crosses the selected threshold. The PVD can be enabled in all modes except Standby modes. 7 thresholds can be selected by software. In addition, comparisons can be done with an external pin.

The analog VDDA supervisor handles voltage detection via the analog voltage detector (AVD) when VDDA crosses the selected threshold. The AVD can be enabled in all modes except Standby modes. 4 thresholds can be selected by software.

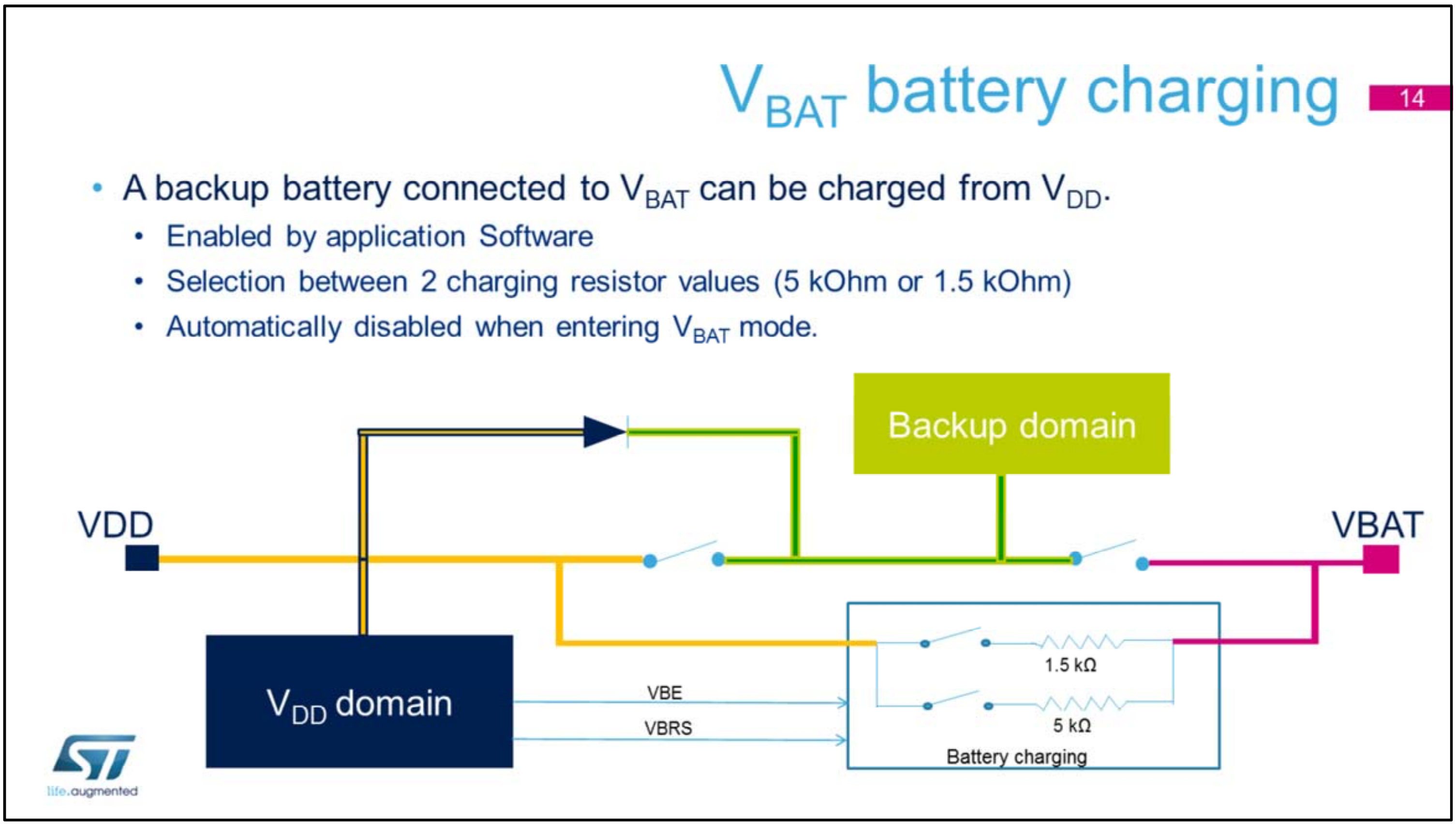
The VBAT supply voltage is monitored to detect when VBAT crosses the minimum and maximum thresholds. The VBAT voltage detection function can be enabled in all modes.
The main VCORE supervisor handles reset management and over-voltage detection.
The Backup domain VSW supervisor handles reset management when the supply drops below the operating level.
The Backup regulator VBKP supply supervisor verifies that the regulator is ready to supply the backup RAM, before entering Standby mode.
The step-down convertor VFBSMPS supply supervisor verifies that the converter ready and the supply is at the selected level.
The USB interface VDD33USB supply supervisor verifies that the USB interface supply is present. The USB supervision can be enabled in all modes except Standby modes.
The DSI regulator VCAPDSI supply supervisor verifies that the DSI regulator is ready to supply the DSI interface.



The V_{DD} power supply supervisor guarantees a safe and ultra-low power reset management.
STM32H7 devices embed an ultra-low-power brown-out reset (BOR) which is always enabled in all power modes. The BOR ensures reset generation as soon as the MCU drops below the selected threshold, regardless of the V_{DD} slope. Four thresholds from 1.62 to 2.78 V are selected by option byte programmed in Flash memory.
The BOR consumption with the 1.7 V threshold is indicated in the datasheet.



The temperature supervisor detects when the junction temperature crosses the minimum and maximum thresholds. The temperature detection function can be enabled in all modes.



The battery charging feature can charge a super-cap connected to the VBAT pin through an internal resistor when the V_{DD} supply is present. The charging is enabled by software and is done either through a 5k Ohm or 1.5 kOhm resistor depending on software. Battery charging is automatically disabled in VBAT mode.

System definition

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Dynamic sub-system configuration for optimized consumption

- The system allows to configure the environment for its sub-system:
  - CPU1 (Cortex M7)
  - CPU2 (Cortex M4)
  - D3 autonomous
- The system is configurable based on peripheral allocation
  - A CPU sub-system is composed of the:
    - CPU and associated domain bus matrix
    - D3 domain bus matrix
    - Bus matrix fixed peripherals
    - Allocated peripheral with associated domain bus matrix (PERxEN)
  - The D3 domain autonomous mode is composed of the:
    - D3 domain bus matrix
    - Autonomous mode allocated peripherals (PERxAMEN). Autonomous mode peripherals need also to be allocated by a CPU sub-system.

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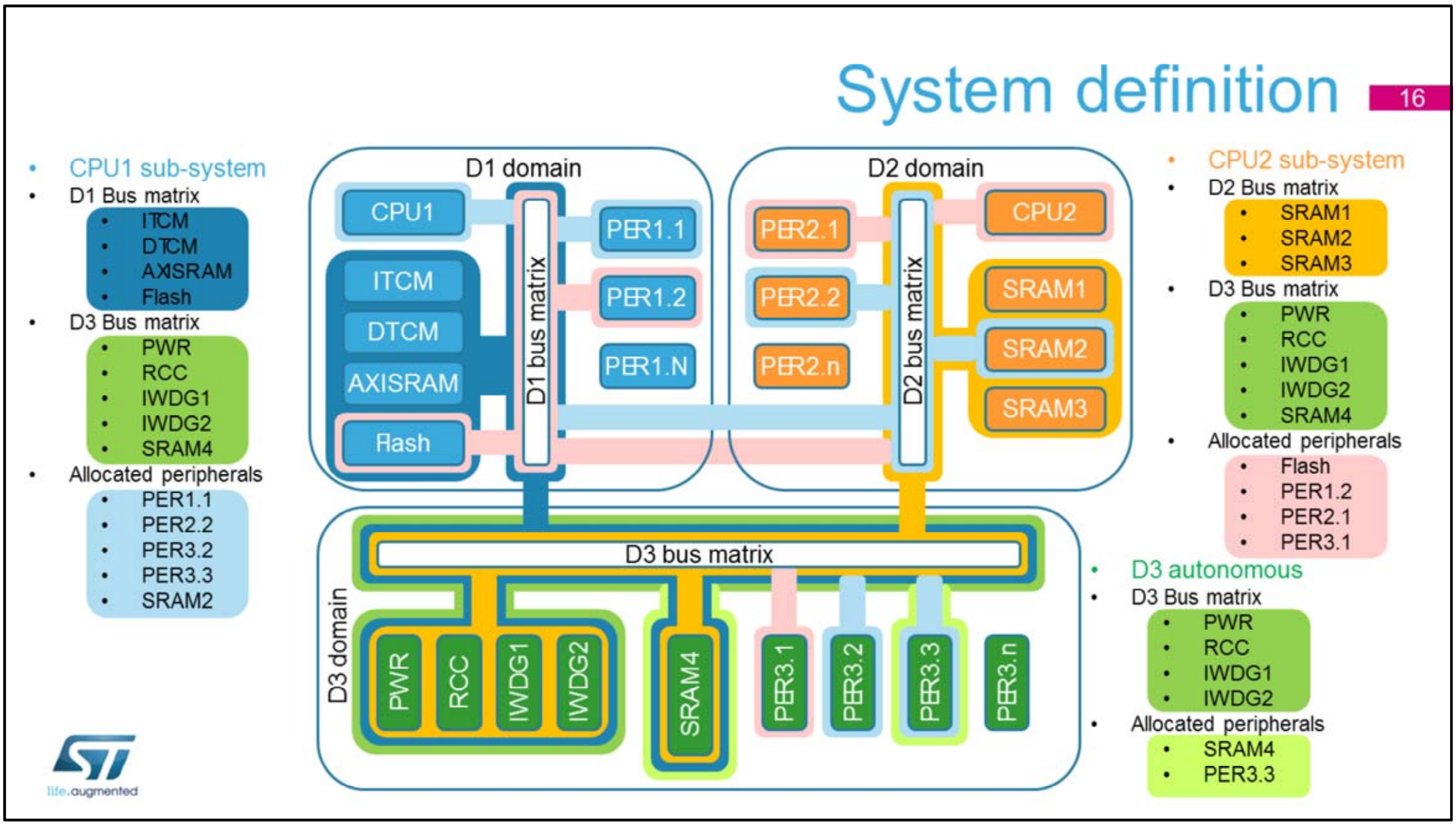
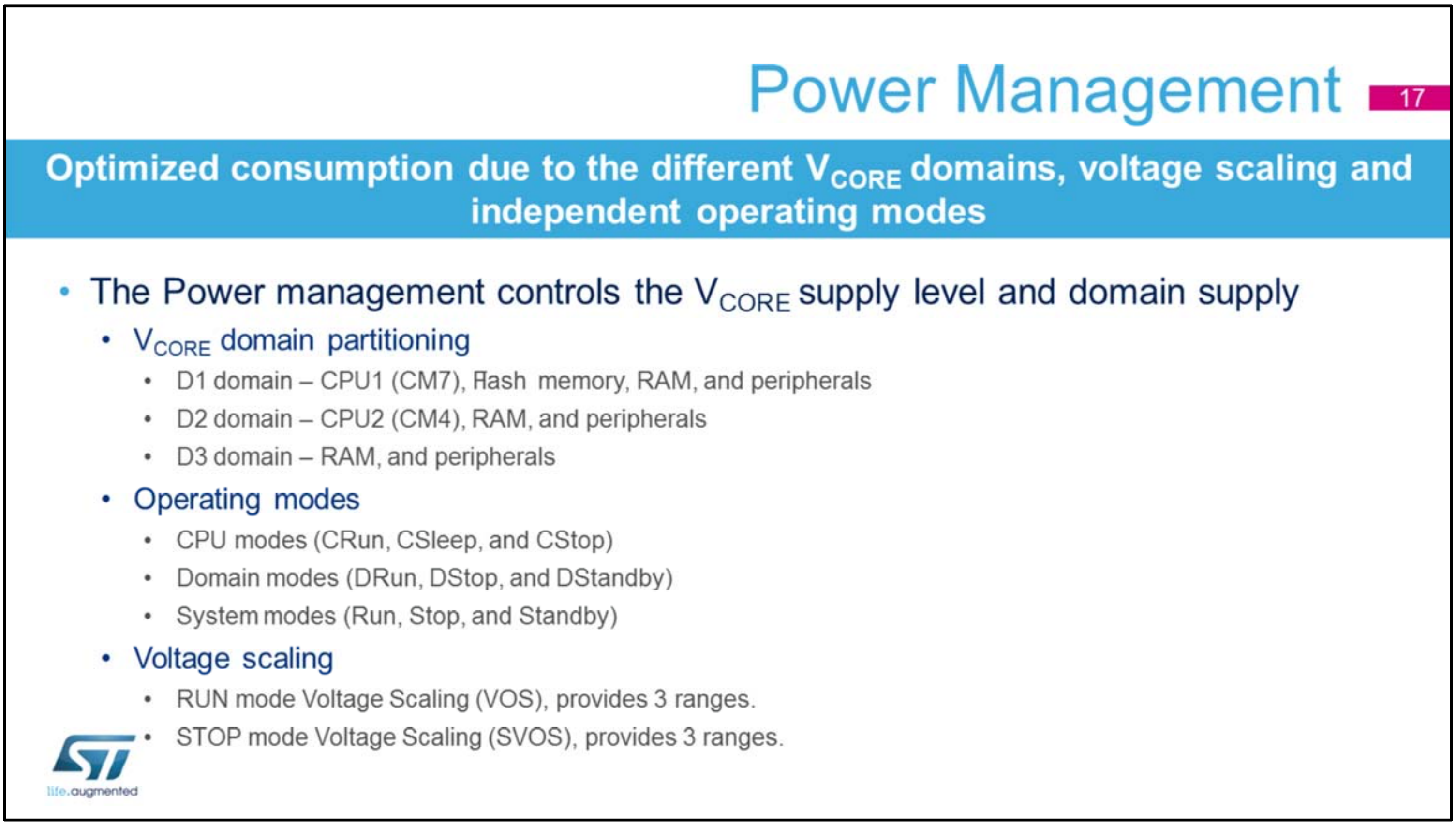
By allocating peripherals to a CPU or the D3 autonomous mode, the boundary of the sub-system can be controlled. The sub-system will follow its associated CPU or D3 autonomous mode operating mode. This is used to optimize the sub-system's power consumption.
Peripheral allocation is done in the RCC via the PERxEN and PERxAMEN register bits, enabling the automatic wakeup of the domains associated with the woken-up sub-system.



When CPU1 is in CRUN mode, the fixed allocated D1 bus matrix and D3 bus matrix peripherals are clocked. Other peripherals may be allocated when needed. When allocating a peripheral in the D2 domain, the D2 domain will be powered and the D2 bus matrix with its fixed peripherals and the CPU1 allocated peripheral(s) will be clocked.
When CPU2 is in CRUN mode, the fixed allocated D2 bus matrix and D3 bus matrix peripherals are clocked. Other peripherals may be allocated when needed. When allocating a peripheral in the D1 domain, the D1 domain will be powered and the D1 bus matrix with its fixed peripherals and the CPU2 allocated peripheral(s) will be clocked.
When D3 is in Autonomous run mode, the fixed allocated D3 bus matrix peripherals and the D3 domain Autonomous mode allocated peripherals are clocked.



Power management functions control the power supply for the different domains based on the domain operating mode. The system and domain operating mode depend on the CPU operating mode and the CPU's sub-system boundaries.

Voltage scaling modes

Flexibility between required performance and consumption

Voltage range	Mode	SYSCLK	CM7	CM4	D2/D3 domain	Stop mode Wakeup Peripheral
Range 0	Run	480 MHz max	480 MHz	240 MHz	240 MHz	Kernel clock on
Range 1	Run	400 MHz max	400 MHz	200 MHz	200 MHz	
Range 2	Run	300 MHz max	300 MHz	150 MHz	150 MHz	
Range 3	Run	200 MHz max	200 MHz	100 MHz	100 MHz	
	Stop	off	off	off	off	
Range 4	Stop					off
Range 5	Stop					

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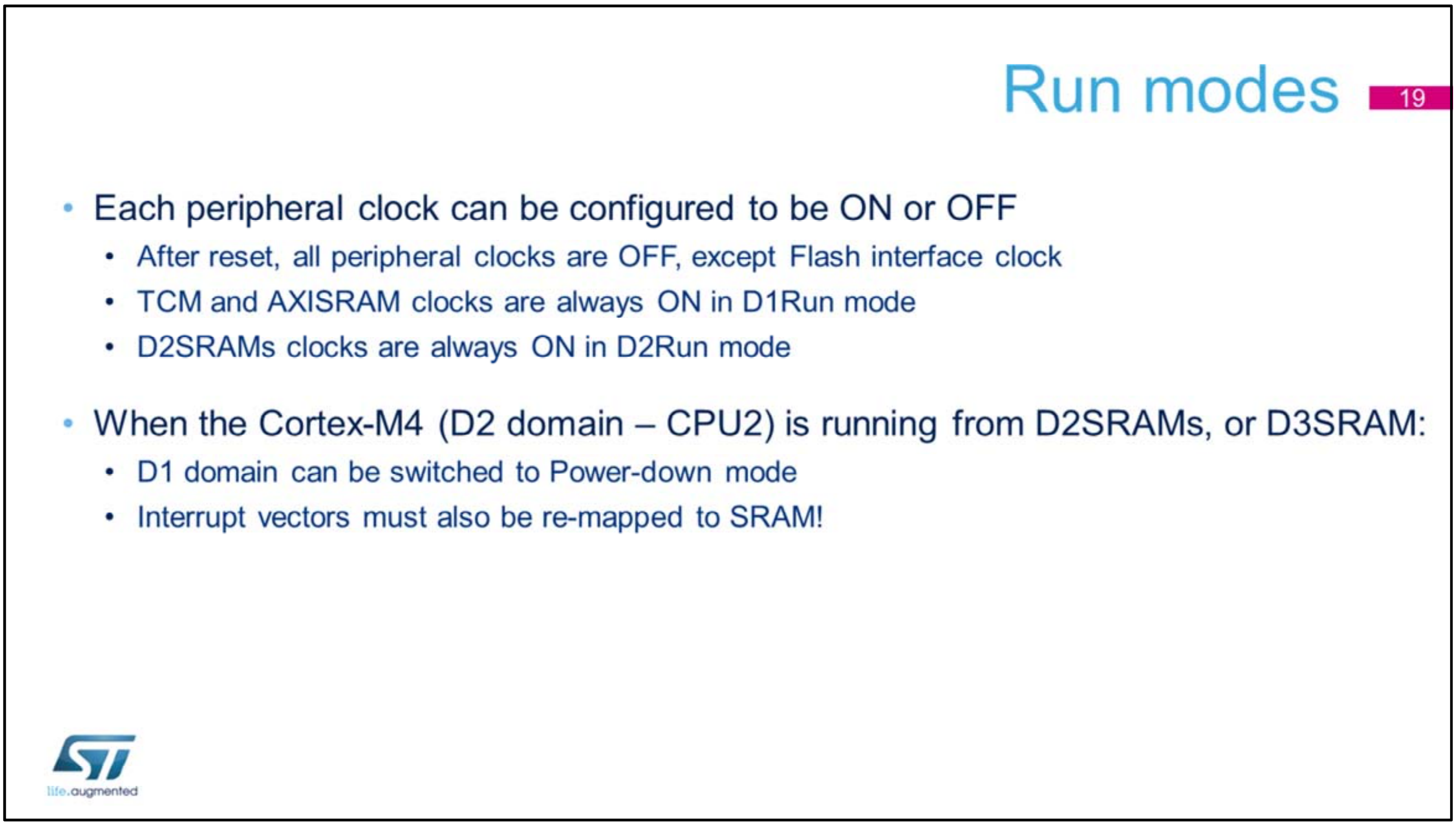
Thanks to voltage scaling, the various Run modes offer flexibility between the required performance and consumption.
In Run Mode Range 0 (enhanced performance with high power consumption), the system clock is limited to 480 MHz.
In Run Mode Range 1 (high performance with high power consumption), the system clock is limited to 400 MHz.
In Run Mode Range 2 (medium performance and power consumption), the system clock is limited to 300 MHz.
In Run Mode Range 3 (low performance with low power consumption), the system clock is limited to 200 MHz.
The internal and external oscillators as well as the PLL can be used in all modes, respecting the maximum frequencies.
The Run mode range is determined by the system clock frequency even when a CPU is in CStop mode.
In Stop Mode Range 3, the peripherals with wakeup from Stop mode capabilities (UART, SPI, I2C, and LPTIM) are operational.
In Stop Mode Ranges 4 and 5, the peripherals with wakeup from Stop mode capabilities are disabled.



Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes. By default all peripherals clocks are OFF, except the Flash interface clock. The SRAM clocks are enabled in Run mode.

When running from D1SRAM, D2SRAM or D3SRAM, the Flash memory can be put in Power-down mode thanks to software, and the Flash clock can be switched off. The Flash memory must not be accessed when it is switched off, consequently interrupts must be mapped in SRAM, using the Cortex-M Vector Table Offset Register.

CPU operating modes

Mode	Description
CRun	CPU Active ➔ CPU, CPU-sub system bus matrix(s), CPU enabled peripheral clock(s) active.
CSleep	CPU Sleep ➔ CPU clock stopped, CPU-sub system bus matrix(s), CPU sleep enabled peripheral clock(s) active.
CStop	CPU Deepsleep ➔ CPU, CPU-sub system bus matrix(s), CPU peripheral clock(s) stopped.

- CPU operating modes are directly controlled from the CPU
  - Entering low power modes
    - CSleep is entered by executing WFI/WFE or on return from ISR. (DEEPSLEEP = 0)
    - CStop is entered by executing WFI/WFE or on return from ISR. (DEEPSLEEP = 1)
  - Exiting low power modes
    - When low-power mode was entered by WFI or return from ISR
      - on any CPU interrupt with sufficient priority
    - When low-power mode was entered by WFE
      - on CPU event
      - SVONPEND = 0 ➔ on interrupts with sufficient priority
      - SVONPEND = 1 ➔ on any interrupt

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The CPU entering low power mode is controlled by the Cortex-M WFI and WFE, and the DEEPSLEEP bit allows to select between CSleep and CStop mode.
When the CPU enters CStop mode, the domain and system operating mode depend on the other CPU and the D3 autonomous modes.
A CPU NVIC interrupt with sufficient priority will wake up the CPU after a WFI or return from ISR.
A CPU event input (rxev) will wake up the CPU after a WFE. In addition when the Cortex-M SVONPEND bit is clear, an NVIC interrupt with sufficient priority will wake up the CPU after a WFE. When the SVONPEND bit is set, any NVIC interrupt will wake up the CPU after a WFE.

Domain operating modes

Mode	Description
DRun	Domain bus matrix, clock active.
DStop	Domain bus matrix and domain peripheral clock(s) stopped.
DStandby	Domain powered down.

- D1 & D2 domain operating modes are controlled from the CPUs having allocated peripherals in the domain.
  - The domain is in:
    - DRun when a CPU with allocated domain peripherals is in CRun or Csleep mode
    - DStop when the CPU(s) with allocated domain peripherals is(are) in CStop mode and at least one domain PDDS_Dn bit selects Stop
    - DStandby when the CPU(s) with allocated domain peripherals is(are) in CStop mode and all domain PDDS_Dn bits select Standby

Power management functions control the power supply for the different domains based on the CPU operating mode and the domain Power Down Deepsleep selection through the PWR register bits PDDS_Dn. Each CPU has its own control bits for the 3 domains.
A domain will only enter DStop mode when the domain CPU is in CStop mode and the other CPU has no allocated peripherals or is also in CStop mode.

System operating modes

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Mode	Description
Run	System clock is active and forwarded to the system.
Stop	System clock is stopped.
Standby	System is powered down. (Backup domain may be kept active)

- System operating modes controlled from the CPUs and wakeup sources.
  - Run when a CPU is in CRun or CSleep mode or a wakeup source is active.
  - Stop when the CPUs are in CStop mode and all wakeup sources are cleared and D3 domain is not forced in Run mode, and at least one PDDS_Dn bit selects Stop.
  - Standby when the CPUs are in CStop mode and all wakeup sources are cleared and D3 domain is not forced in Run mode, and all PDDS_Dn bits select Standby.
- The System supports an D3 autonomous RUN mode:
  - A peripheral in the D3 domain needs to be enabled for Autonomous mode.
  - A CPU forces the D3 domain to stay in Run mode via its RUN_D3 register bit

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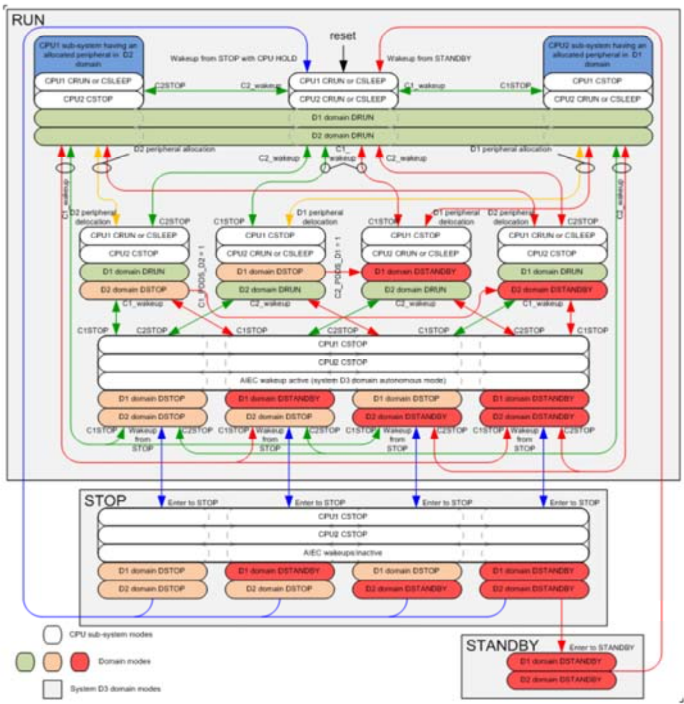
The STM32H7 system (D3 domain) operating mode is controlled from both CPUs and the D3 autonomous mode.
The system will only enter Stop or Standby mode when both CPUs are in CStop mode and there is no active wakeup source or if the D3 domain is forced in Run mode.
The system will only enter Standby mode when the Power Down Deepsleep selection in PWR register bits PDDS_Dn allows all domains to enter Standby mode.
The D3 autonomous mode can set the system in Run mode, either by a CPU forcing the D3 domain in Run mode via its RUN_D3 register bit, or by a peripheral wakeup source request.

System power control states

- System power state is controlled from both CPUs and the D3 domain.
- State transitions may be initiated by:
  - a CPU going to low-power mode.
    - CPU, Domain and System modes
  - a peripheral allocation / de-location
    - Domain mode
  - a wakeup event
    - CPU, Domain and System modes
  - changing PDDS setting to Standby
    - Domain mode



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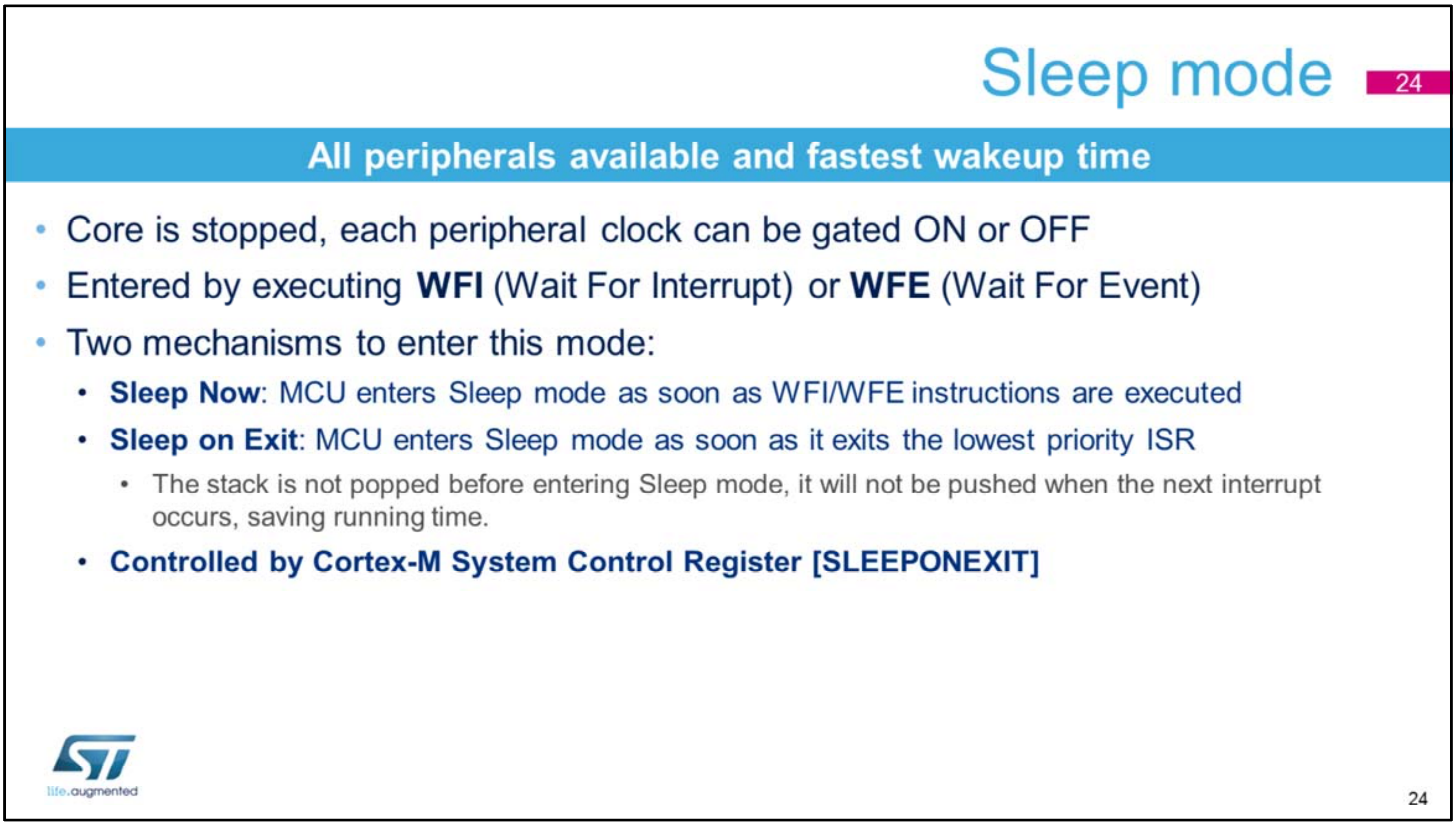
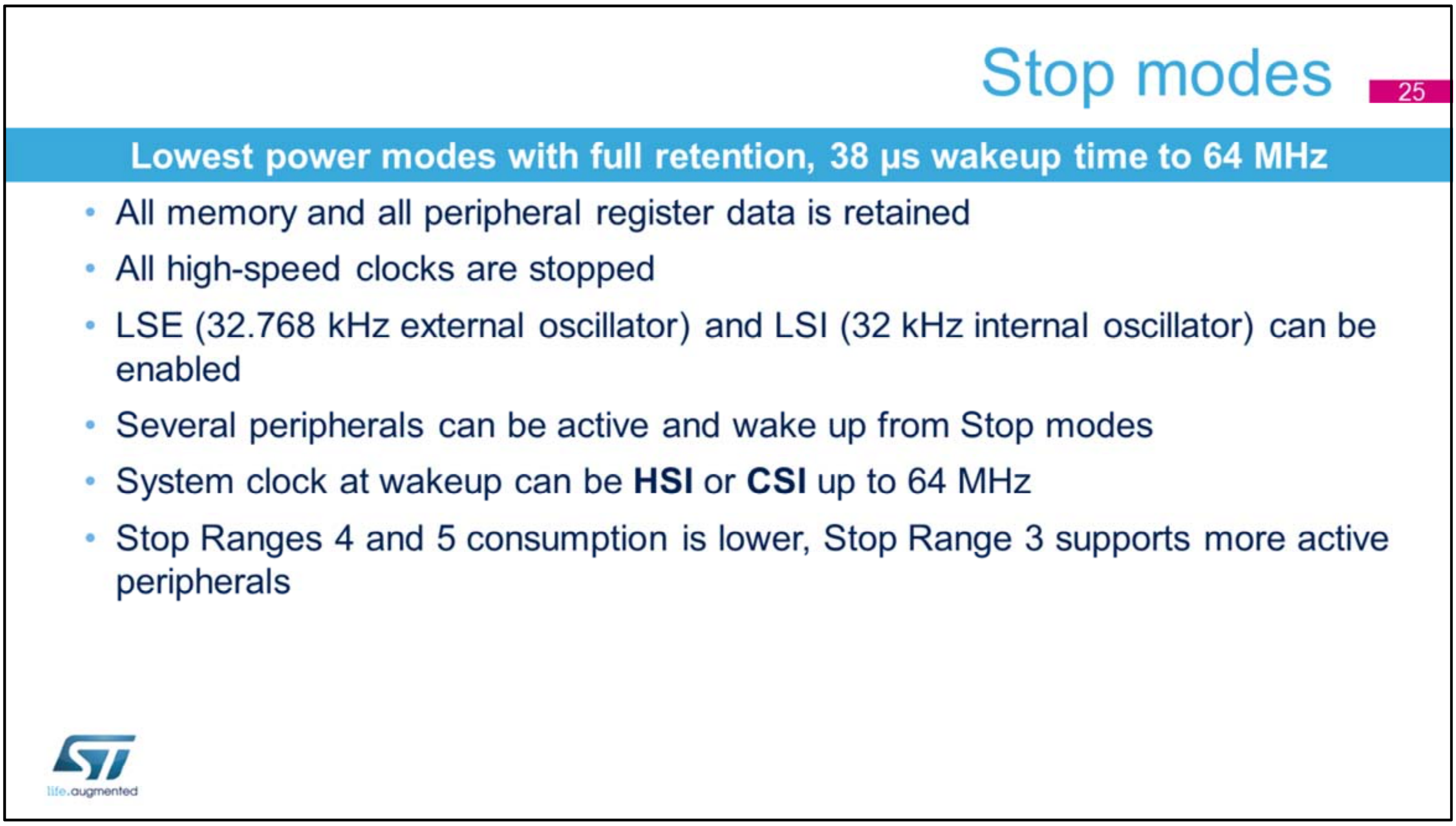
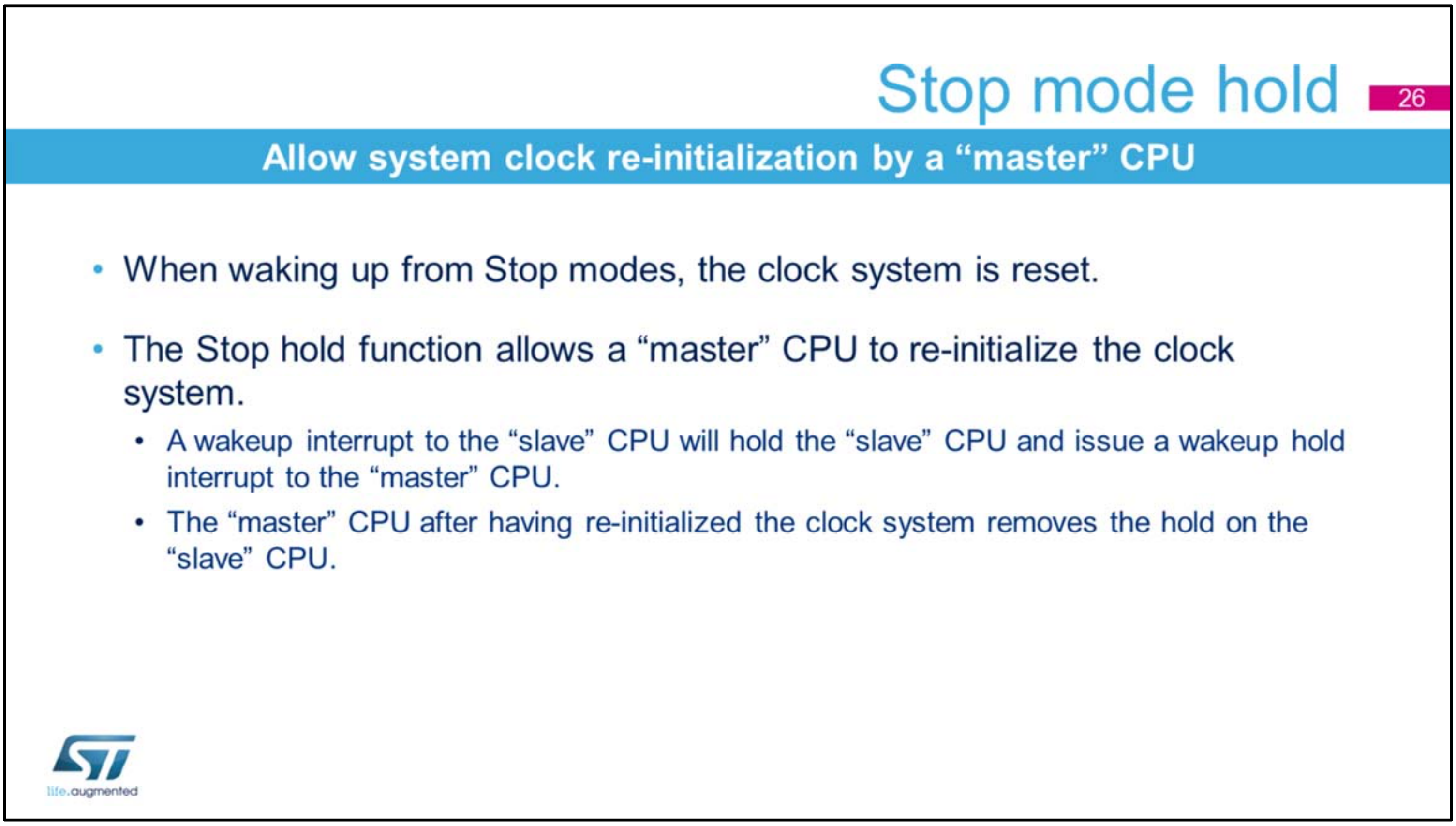
This figure gives the complete overview of the power modes in relation to the CPU operating modes and the D3 autonomous mode.



Sleep and Low-power sleep modes enable all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes.
These modes are entered by executing the assembler instruction Wait for Interrupt or Wait for Event. When executed in Low-power run mode, the device enters Low-power sleep mode.
Depending on the SLEEPONEXIT bit configuration in the CortexM4 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine. This last configuration saves time and consumption by removing the need to pop and push the stack.



STM32H7 devices features three Stop modes: Stop range 3, range 4 and range 5, which are the lowest power modes with full retention and fast wakeup time to Run mode **at 64 MHz**.
The contents of SRAMs and all peripherals registers are preserved in all Stop modes.
All high speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up can be the internal high-speed and Low-power (CSI) oscillators up to 64 MHz with only a 12 µs from FLASH.
Stop range 4 and Range 5 consumption is lower than Stop Range 3, but support less active wakeup peripherals.



To be able to re-initialize the clock system by a so called "master" CPU, when exiting from Stop modes, the Stop hold function holds the so-called "slave" CPU until the "master" CPU has re-initialized the system. To do this, a "slave" CPU wakeup from Stop mode interrupt will hold the "slave" CPU and wake up the "master" CPU with a wakeup hold interrupt. Once the "master" CPU has re-initialized the system, it clears the "slave" CPU hold, where afterwards the "slave" CPU will receive the initial wakeup interrupt.

Stop modes comparison

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	Stop Range 3	Stop Range 4	Stop Range 5
Consumption	25 °C, 3,3 V		
	350 µA	220 µA	150 µA
Wakeup time to 64 MHz	12 µs in Flash memory	23 µs in Flash memory	38 µs in Flash memory
Wakeup clock	**HSI up to 64 MHz** or **CSI** at **4 MHz**		
Regulator	Regulator Main mode	Regulator Low power mode	
Peripherals	LPTIM, RTC, I/Os, BOR, PVD, AVD, COMPs, and IWDG		
	Other peripherals allowing wakeup from Stop mode	None	

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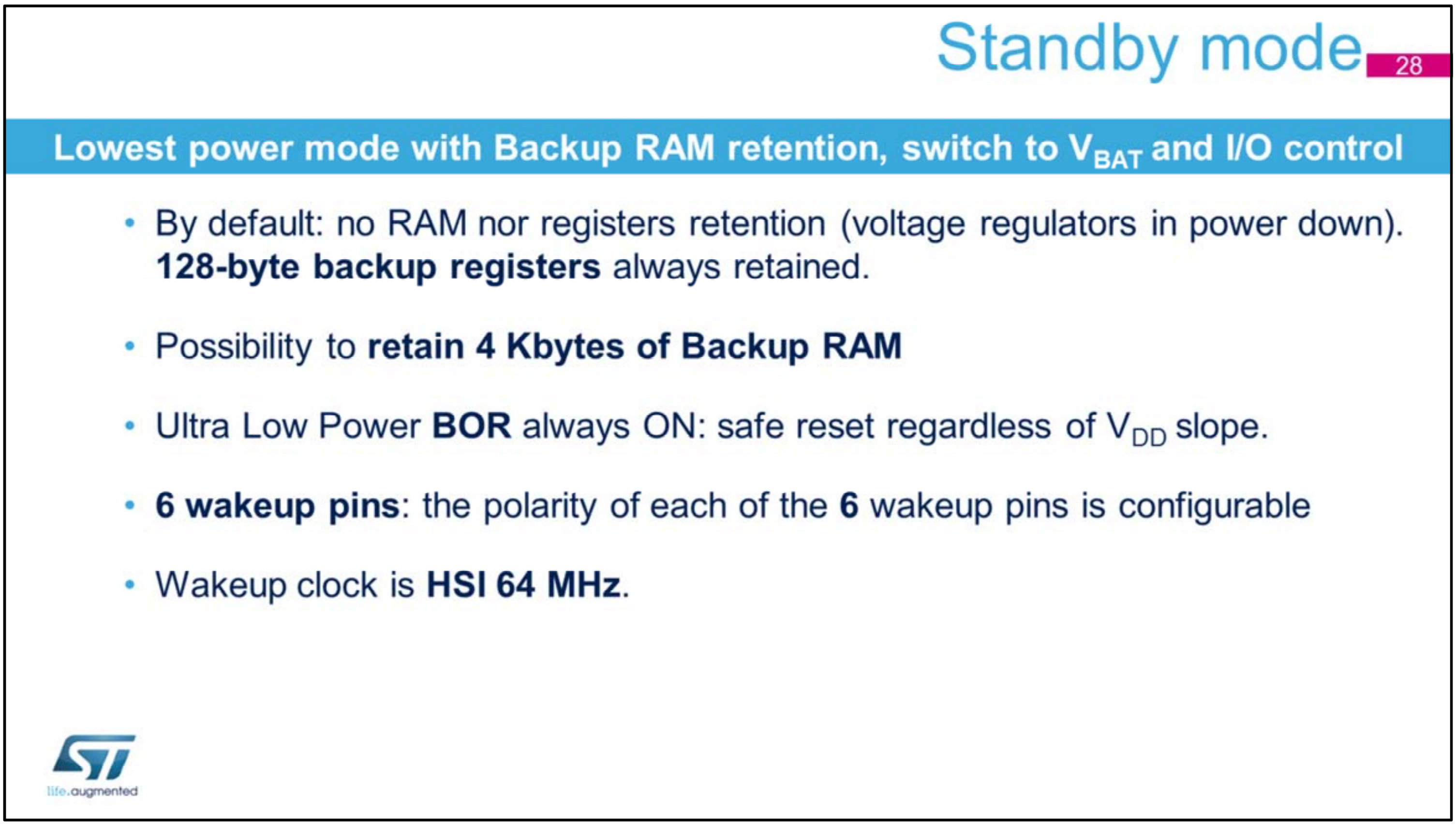
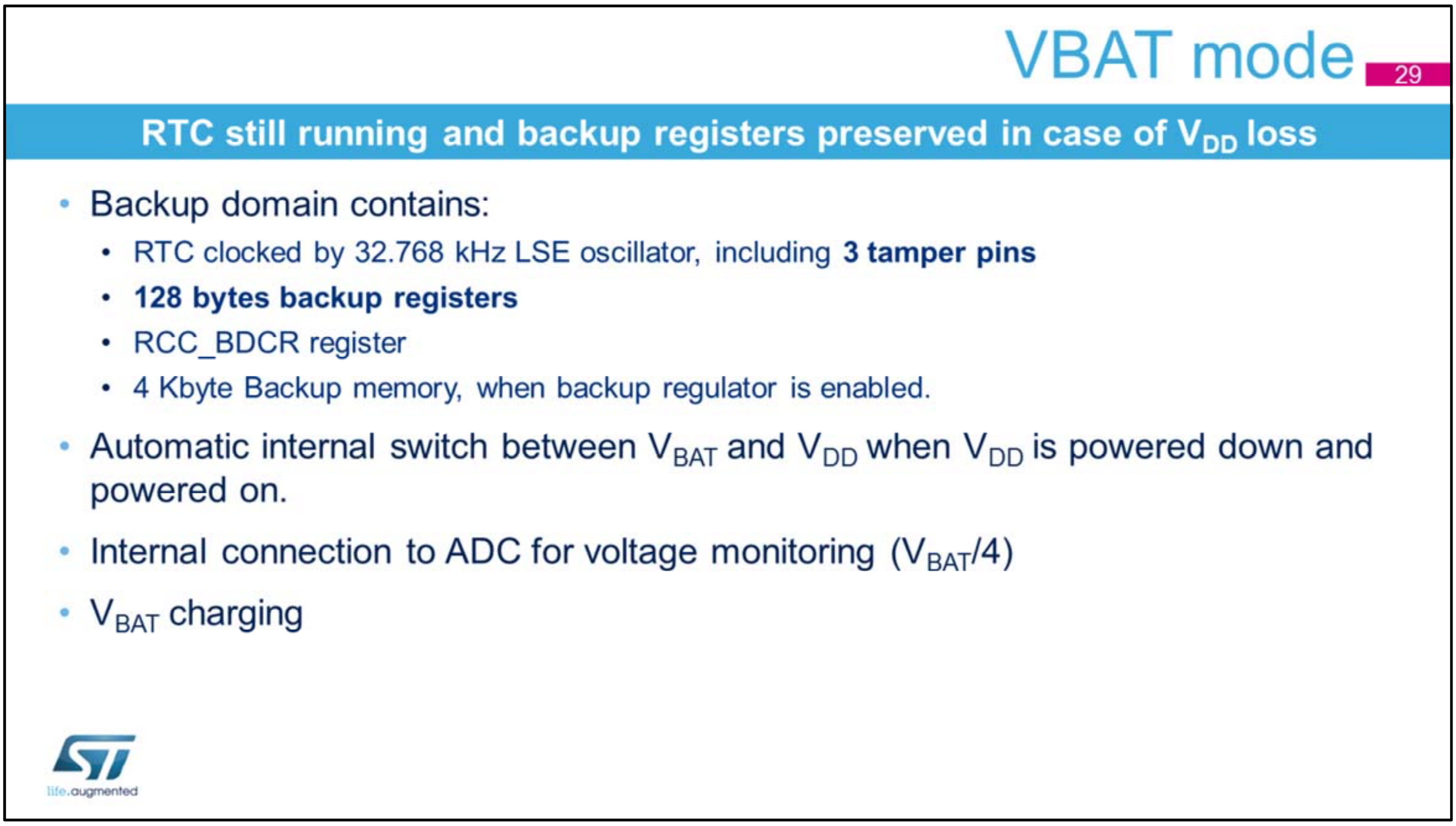
When comparing Stop modes:
Stop Range 3 consumption is higher than Stop Ranges 4 and 5, but the wakeup time is shorter and the number of active peripherals is higher.
Stop Range 3 keeps the V_{CORE} domain at the same supply level as Run Range 3, allowing a very short wake-up time lower than 12 µs when restarting from the RAM to the expense of a higher consumption than Stop mode with Ranges 4 and 5.
It is possible to wake up from Stop Range 3 with peripherals supporting wakeup from Stop mode (UART, SPI, I2C, and LPTIM).



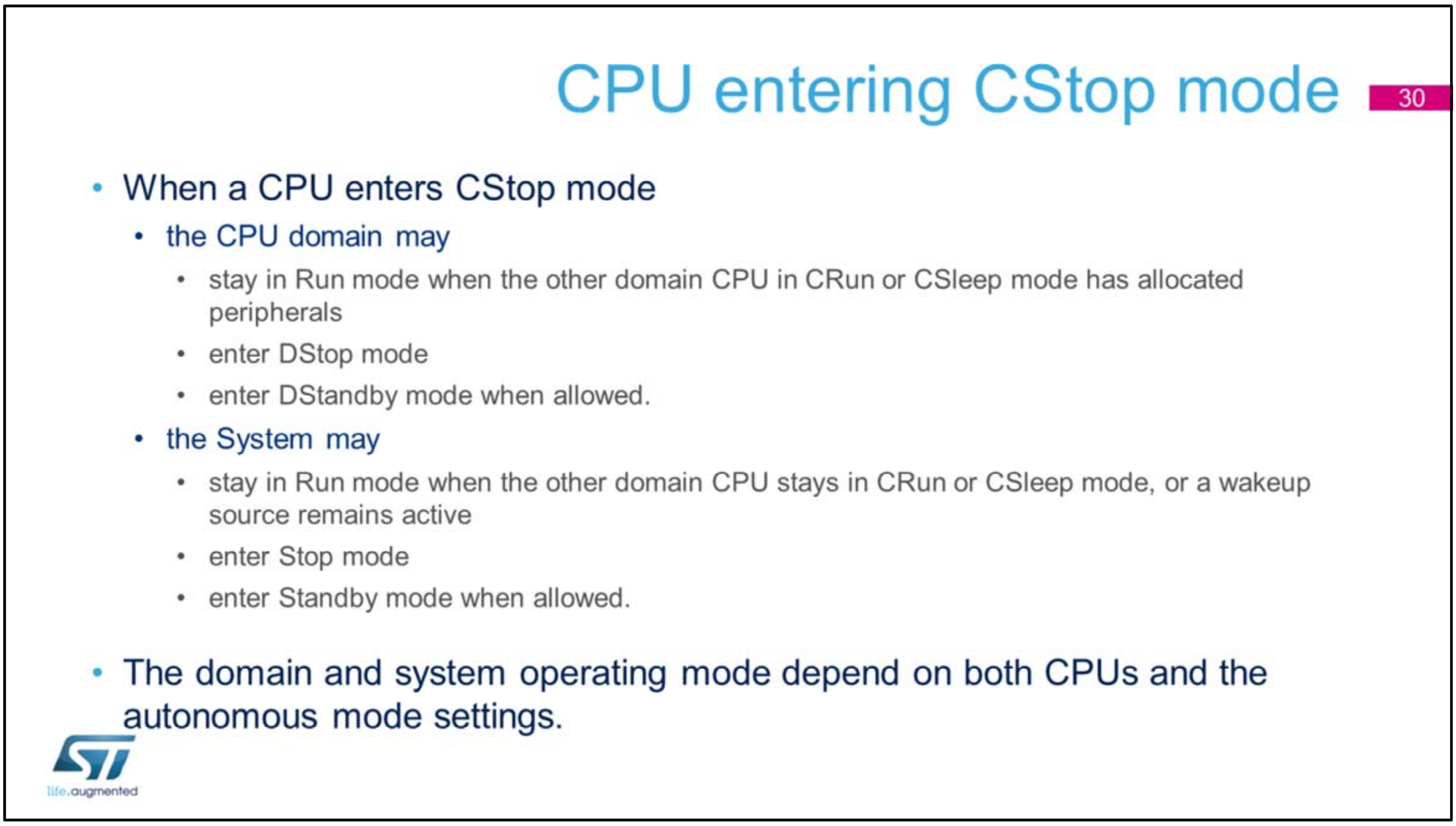
The Standby mode is the lowest power mode in which 4 Kbytes of Backup RAM can be retained, the automatic switch from VDD to VBAT is supported and the I/Os level can be configured by independent pull-up and pull-down circuitry.
By default, the voltage regulators are in Power down mode and the SRAMs and the peripherals registers are lost. The 128-byte backup registers are always retained.
Thanks to software, it is possible to retain 4 Kbytes of Backup RAM.
The ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the VDD slope.
Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bit. This allows control of the inputs state of external components even during Standby mode.
6 wakeup pins are available to wake up the device from Standby mode. The polarity of each of the 6 wakeup pins is

configurable.
The wakeup clock is HSI with a frequency of 64 MHz.



The backup domain allows us to keep the RTC functional and to preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin.
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz. 3 tamper pins are functional in VBAT mode, and will erase the 128-byte backup registers also included in the VBAT domain, in case of intrusion detection.
The backup domain also contains the RTC clock control logic.
In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT. When VDD is back to normal, the backup domain power supply automatically switches back to VDD.
The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery level.
When VDD is present, the battery connected to VBAT can

be charged from the VDD supply.



A CPU will enter CStop mode when executing a WFI or WFE with the DEEPSLEEP bit set. The domain and system state will also depend on the other CPU's operating mode and wakeup source status. Only when the other CPU has no allocated peripherals in the domain or the other CPU is also in CStop mode, the domain may enter DStop or DStandby mode. When in addition none of the wakeup sources is active, the system may enter Stop or Standby mode.

CPU wakes up from CStop mode

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- To know from which domain and system low-power mode the CPU wakes up from CStop mode, flags are provided.
  - SBF_Dn
    - CPU domain has woken up from DStandby mode (The system may have stayed in Run mode or have been woken up from Stop mode)
      - CPU starts from reset
  - STOPF
    - System has woken up from Stop mode
      - Wakeup interrupt to the CPU will be pending in AIEC or peripheral
  - SBF
    - System has woken up from Standby mode
      - CPU starts from reset, there is no wakeup interrupt pending in the AIEC.

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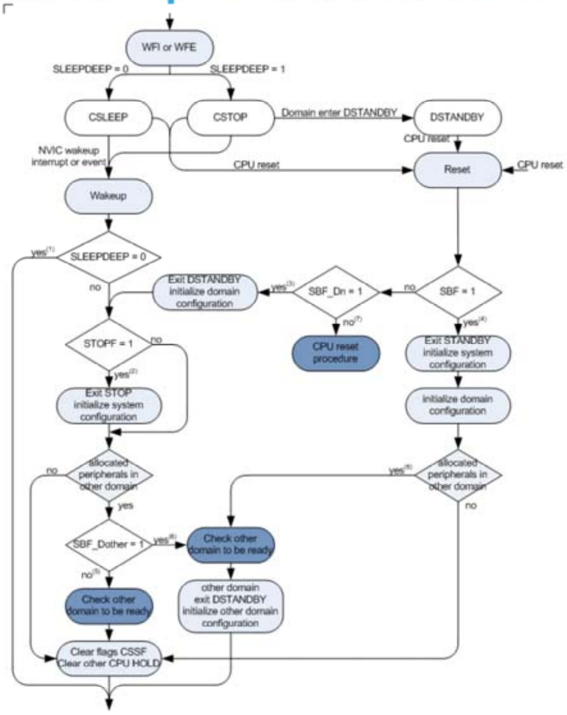
When a CPU wakes up from its CStop mode, it has to know from which mode the domains and system have woken up. For this, the CPU has dedicated flag bits SBF_D1, SBF_D2, SBF and STOPF. These bits inform the CPU about the state of the system, and which parts may need to be reinitialized.

Software low-power procedure

- The Low-power mode to enter is configured by:
  - The Cortex-M SLEEPDEEP bit
    - Sleep or Other low power modes
  - and the PWR Domain PDDS bits.
    - STOP or STANDBY
- To know from which low-power mode the CPU is woken up, the following bit must be checked:
  - The Cortex-M SLEEPDEEP bit
    - Sleep
  - PWR control
    - STOPF
    - Domain SBF_D1 and SBF_D2.
    - System SBF



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The Cortex-M SLEEPDEEP bit allows selection of the CPU to enter CSleep or CStop modes.
When the CPU enters CStop mode, the PWR control bits PDDS_D1, PDDS_D2, and PDDS_D3 select which state the Domains may enter in. The state of the domains depend also on the other CPU’s sub-system configuration and operating mode and the wakeup source status.
From CSleep mode, the CPU will always wake up through an interrupt or event. In this case, the Cortex-M DEEPSLEEP bit is 0.
From CStop mode, the CPU may wake up through an interrupt or via a reset depending on the domain state.
If the domain was in DStop mode, the CPU woke up through an interrupt. In this case, the Cortex-M DEEPSLEEP bit is 1. When in addition the STOPF bit is 0, the system remained in Run mode, so there is no need to re-initialize the clock system.
If the STOPF bit is also set, it means that the system woke

up from Stop mode and the clock system needs re-initialization. If the CPU has allocated peripherals in the other domain, check the other domain’s SBF_Dn flag to know if the domain was in DStandby mode. In this case, the peripheral in the other domain needs to be reinitialized.
If the domain was in DStandby mode, the CPU will wake up through a reset. If the SBF flag is also set, the system was in Standby. In this case a full system initialization is need. When the SBF flag is 0 and the CPU domain SBF_Dn flag is set, the system remained either in Run or Stop mode and only the CPU domain has exited from DStandby. In this case, only the CPU and its domain need to be re-initialized, afterwards the system state must be checked to know if the system remained in Run mode or was in Stop mode.
When the CPU domain SBF_Dn flag doesn’t indicate DStandby, the CPU woke up via a system POR reset.

Wakeup

- The CPU wakeup state depends on the domain and system state

CPU mode	Domain mode	System Mode	SBF_Dn	SBF	STOPF	CPU wakeup to RUN	System clock
CSleep	DRun	Run	0	0	0	By NVIC interrupt or event.	Unchanged
CStop	DRun	Run	0	0	0	By EXTI wakeup interrupt through NVIC, or event.	Unchanged
CStop	DStop	Run	0	0	0	By EXTI wakeup interrupt through NVIC, or event.	Unchanged
CStop	DStop	Stop	0	0	1	By EXTI wakeup interrupt through NVIC, or event.	Default after Stop
CStop	DStandby	Run	1	0	0	By EXTI wakeup via reset	Unchanged
CStop	DStandby	Stop	1	0	1	By EXTI wakeup via reset	Default after Stop
CStop	DStandby	Standby	0	1	0	By WKUP wakeup via reset	Reset after Standby
Any	Any	Any	0	0	0	By POR via reset	Default after reset

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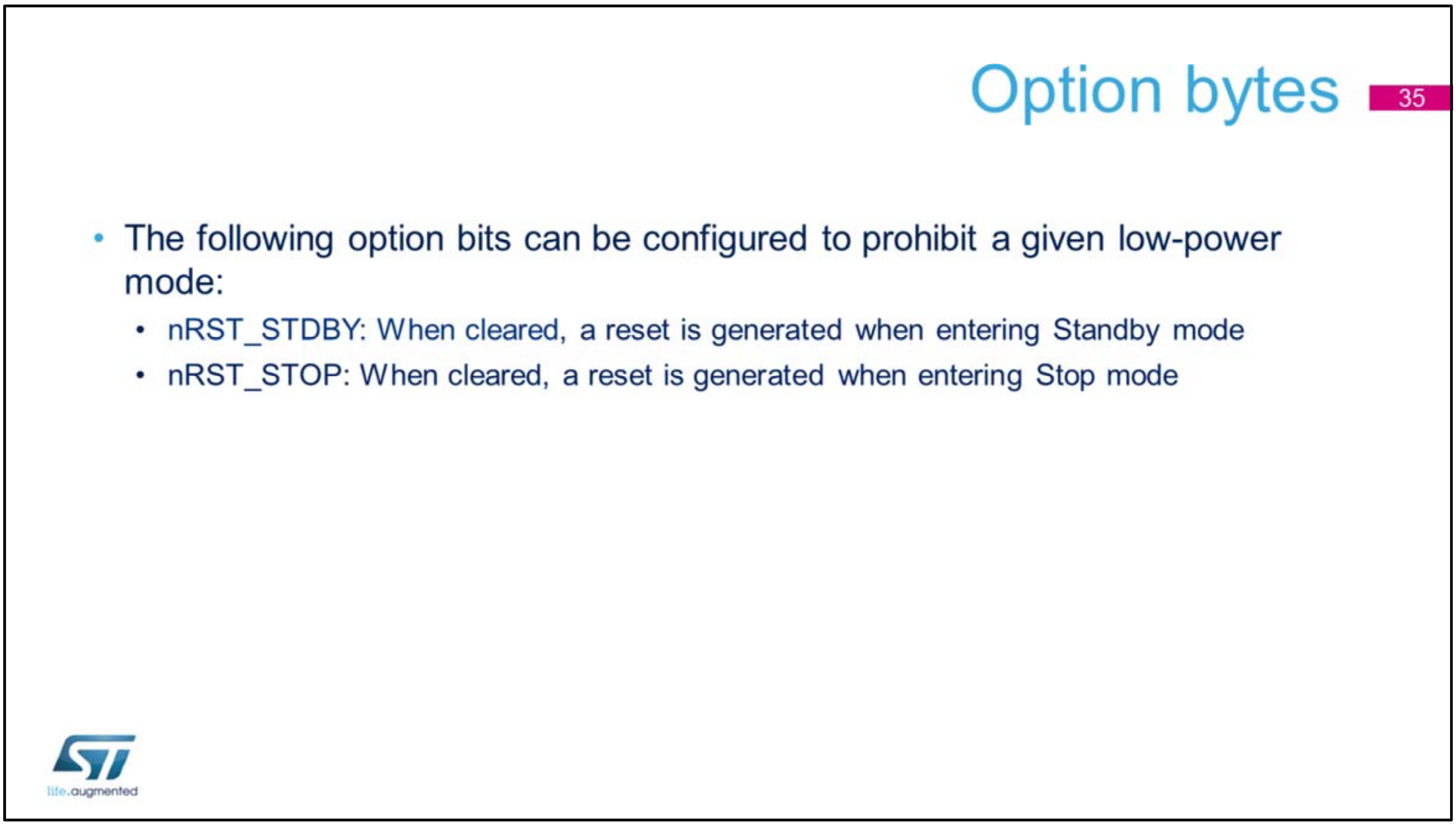
This table gives an complete overview of the CPU, domain and system mode and the wakeup flag bits. It also shows how the CPU was awaken, through an interrupt or an event, or a CPU reset.

PWR interrupts

Interrupt event	Description	Availability
WKUP[6:1]	Wakeup from Standby mode. Wakeup from Stop mode via event signal to EXTI	Run, Stop and Standby
PVDO	Wakeup from Stop mode via event signal to EXTI	Run and Stop
AVDO	Wakeup from Stop mode via event signal to EXTI	Run and Stop
VBATH, VBATL	Wakeup from Standby mode & STOP mode via RTC Tamper Interrupt	Run, Stop and Standby
TEMPH, TEMPL	Wakeup from Standby mode & STOP mode via RTC Tamper Interrupt	Run, Stop and Standby

Here a summary of the PWR control related interrupts.



2 bits are available in the Flash option bytes to prohibit entering a given low-power mode. When cleared, these option bits trigger a reset when entering either Standby or Stop modes. This is a security feature used to reduce the impact of unintentional entry into these low-power modes. If these low-power modes are not used in user code, the option should be enabled.

Debug information

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- The DBGMCU_CR register enables debugging in Standby mode:
  - DBG_STANDBY: When set, the digital part is not powered down in Standby mode. When exiting from Standby mode, a reset is generated.
- When DBG_STANDBY is enabled, the connection with the debugger is kept during the Standby mode.
  After wakeup, debugging is still possible.

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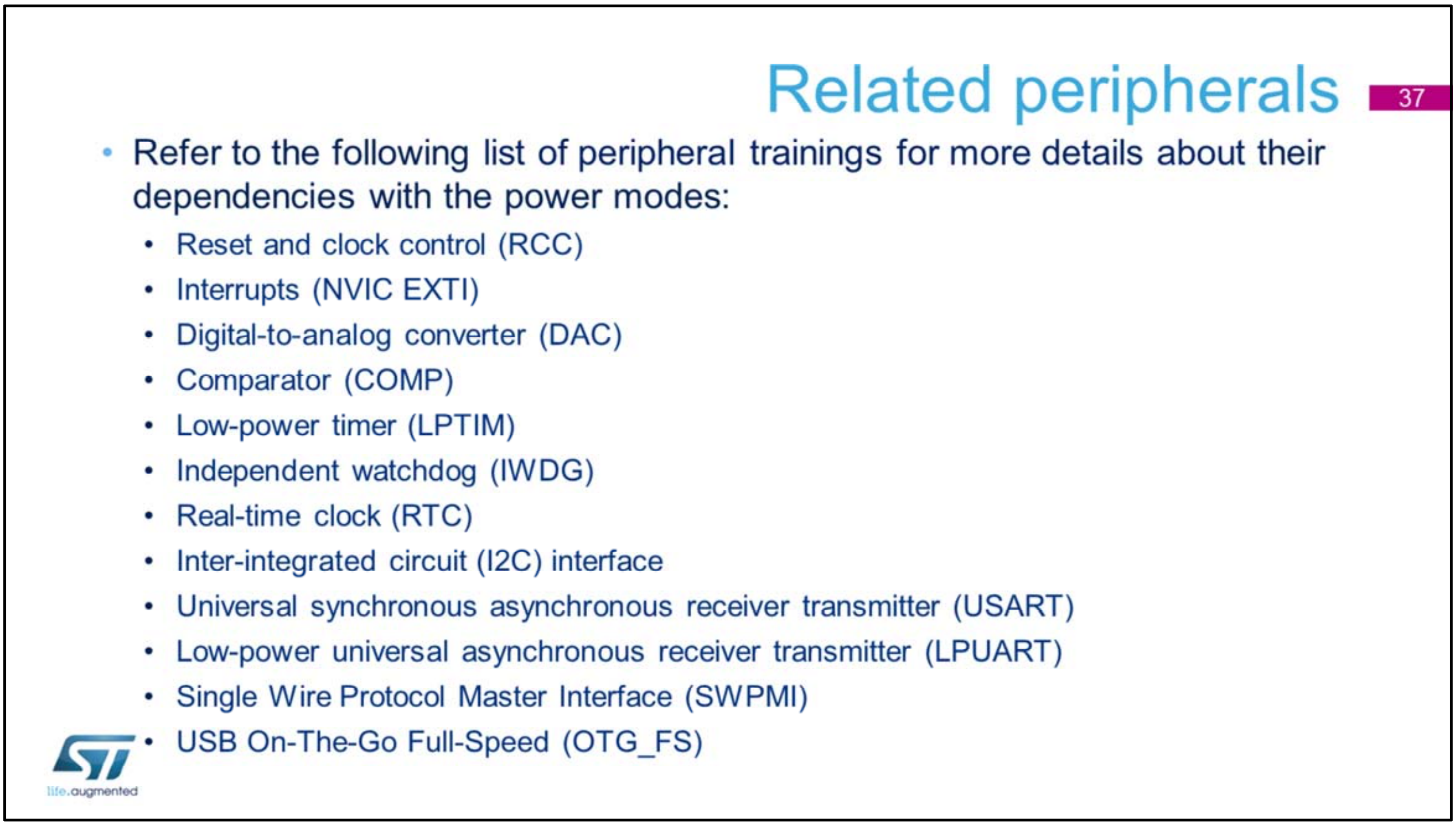
The Debug Control Register is used to enable debugging in Standby mode. When the related bit is set, the regulator is kept ON and the Domains are supplied in Standby modes. This maintains the connection with the debugger during the low-power modes, and continues debugging after wakeup. Remember to clear these bits when the MCU is not under debug, because the consumption is higher in all low-power modes when these bits are set, due to the fact they force the regulators to remain enabled.



In addition to this training, you can refer to the Reset and Clock Control and Interrupts trainings as well as those for all the peripherals with wakeup from Stop and Standby capability.