GPIO Base Address
0x60000300
GPIO RegAddr = PERIPHS_GPIO_BASEADDR+ (OFFSET*4)

NUM	OFFSET	RegAddr	RegName
0	0x0000	0x60000300	GPIO_OUT
1	0x0001	0x60000304	GPIO_OUT_W1TS
2	0x0002	0x60000308	GPIO_OUT_W1TC
3	0x0003	0x6000030C	GPIO_ENABLE
4	0x0004	0x60000310	GPIO_ENABLE_W1TS
5	0x0005	0x60000314	GPIO_ENABLE_W1TC
6	0x0006	0x60000318	GPIO_IN
7	0x0007	0x6000031C	GPIO_STATUS
8	0x0008	0x60000320	GPIO_STATUS_W1TS
9	0x0009	0x60000324	GPIO_STATUS_W1TC
10	0x000a	0x60000328	GPIO_PIN0
11	0x000b	0x6000032C	GPIO_PIN1
12	0x000c	0x60000330	GPIO_PIN2
13	0x000d	0x60000334	GPIO_PIN3

14	0x000e	0x60000338	GPIO_PIN4
15	0x000f	0x6000033C	GPIO_PIN5
16	0x0010	0x60000340	GPIO_PIN6
17	0x0011	0x60000344	GPIO_PIN7
18	0x0012	0x60000348	GPIO_PIN8
19	0x0013	0x6000034C	GPIO_PIN9
20	0x0014	0x60000350	GPIO_PIN10
21	0x0015	0x60000354	GPIO_PIN11

22	0x0016	0x60000358	GPIO_PIN12
23	0x0017	0x6000035C	GPIO_PIN13
24	0x0018	0x60000360	GPIO_PIN14
25	0x0019	0x60000364	GPIO_PIN15
26	0x001a	0x60000368	GPIO_SIGMA_DELTA
27	0x001b	0x6000036C	GPIO_RTC_CALIB_SYNC
28	0x001c	0x60000370	GPIO_RTC_CALIB_VALUE

Signal	BitPos	SW(R/W)
GPIO_BT_SEL	[31:16]	R/W
GPIO_OUT_DATA	[15:0]	R/W
	[31:16]	
GPIO_OUT_DATA_W1TS	[15:0]	WO
	[31:16]	
GPIO_OUT_DATA_W1TC	[15:0]	WO
	[31:22]	
GPIO_SDIO_SEL	[21:16]	R/W
GPIO_ENABLE_DATA	[15:0]	R/W
	[31:16]	
GPIO_ENABLE_DATA_W1TS	[15:0]	WO
	[31:16]	
GPIO_ENABLE_DATA_W1TC	[15:0]	WO
GPIO_STRAPPING	[31:16]	
GPIO_IN_DATA	[15:0]	
	[31:16]	
GPIO_STATUS_INTERRUPT	[15:0]	R/W
	[31:16]	
GPIO_STATUS_INTERRUPT_W1TS	[15:0]	WO
	[31:16]	
GPIO_STATUS_INTERRUPT_W1TC	[15:0]	WO
	[31:11]	
GPIO_PIN0_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN0_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN0_DRIVER	[2]	R/W
	[1]	
GPIO_PIN0_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN1_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN1_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN1_DRIVER	[2]	R/W
	[1]	
GPIO_PIN1_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN2_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN2_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN2_DRIVER	[2]	R/W
	[1]	
GPIO_PIN2_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN3_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN3_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN3_DRIVER	[2]	R/W
	[1]	

GPIO_PIN3_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN4_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN4_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN4_DRIVER	[2]	R/W
	[1]	
GPIO_PIN4_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN5_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN5_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN5_DRIVER	[2]	R/W
	[1]	
GPIO_PIN5_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN6_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN6_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN6_DRIVER	[2]	R/W
	[1]	
GPIO_PIN6_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN7_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN7_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN7_DRIVER	[2]	R/W
	[1]	
GPIO_PIN7_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN8_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN8_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN8_DRIVER	[2]	R/W
	[1]	
GPIO_PIN8_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN9_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN9_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN9_DRIVER	[2]	R/W
	[1]	
GPIO_PIN9_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN10_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN10_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN10_DRIVER	[2]	R/W
	[1]	
GPIO_PIN10_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN11_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN11_INT_TYPE	[9:7]	R/W

	[6:3]	
GPIO_PIN11_DRIVER	[2]	R/W
	[1]	
GPIO_PIN11_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN12_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN12_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN12_DRIVER	[2]	R/W
	[1]	
GPIO_PIN12_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN13_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN13_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN13_DRIVER	[2]	R/W
	[1]	
GPIO_PIN13_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN14_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN14_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN14_DRIVER	[2]	R/W
	[1]	
GPIO_PIN14_SOURCE	[0]	R/W
	[31:11]	
GPIO_PIN15_WAKEUP_ENABLE	[10]	R/W
GPIO_PIN15_INT_TYPE	[9:7]	R/W
	[6:3]	
GPIO_PIN15_DRIVER	[2]	R/W
	[1]	
GPIO_PIN15_SOURCE	[0]	R/W
	[31:17]	
SIGMA_DELTA_ENABLE	[16]	R/W
SIGMA_DELTA_PRESCALAR	[15:8]	R/W
SIGMA_DELTA_TARGET	[7:0]	R/W
RTC_CALIB_START	[31]	R/W
	[30:10]	
RTC_PERIOD_NUM	[9:0]	R/W
RTC_CALIB_RDY	[31]	
RTC_CALIB_RDY_REAL	[30]	
	[29:20]	
RTC_CALIB_VALUE	[19:0]	

Description
BT-Coexist Selection register
The output value when the GPIO pin is set as output.

Writing 1 into a bit in this register will set the related bit in GPIO_OUT_DATA

Writing 1 into a bit in this register will clear the related bit in GPIO_OUT_DATA
SDIO-dis selection register
The output enable register.

Writing 1 into a bit in this register will set the related bit in GPIO_ENABLE_DATA

Writing 1 into a bit in this register will clear the related bit in GPIO_ENABLE_DATA
The values of the strapping pins.
The values of the GPIO pins when the GPIO pin is set as input.

Interrupt enable register.

Writing 1 into a bit in this register will set the related bit in GPIO_STATUS_INTERRUPT

Writing 1 into a bit in this register will clear the related bit in GPIO_STATUS_INTERRUPT

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

0: disable; 1: enable GPIO wakeup CPU, only when GPIO_PIN0_INT_TYPE is 0x4 or 0x5
0: disable; 1: positive edge; 2: negative edge; 3: both types of edge; 4: low-level; 5: high-level

1: open drain; 0: normal

1: sigma-delta; 0: GPIO_DATA

1: enable sigma-delta; 0: disable
Clock pre-divider for sigma-delta.
target level of the sigma-delta. It is a signed byte.
Positvie edge of this bit will trigger the RTC-clock-calibration process.

The cycle number of RTC-clock during RTC-clock-calibration
0: during RTC-clock-calibration; 1: RTC-clock-calibration is done
0: during RTC-clock-calibration; 1: RTC-clock-calibration is done

The cycle number of clk_xtal (crystal clock) for the RTC_PERIOD_NUM cycles of RTC-clock